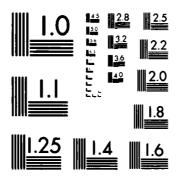
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EMC IN MICROELECTRONICS

Sanders Associates, Inc.

Richard Bossart, John Shekleton and Brian Lessard

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The contents of this report describe a method					
compatibility (EMC) of systems which contain m					
complex digital equipments/devices as contract					
ments/devices. It provides a basis for defini					
and operation of microelectronic systems and s					
magnetic environment. A methodology is establ					

magnetic environment. A methodology is established which describes a stepby-step procedure for assessing EMC in microelectronics and for applying

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the performance criteria. An application of the methodology to a small subsystem is provided to assess the effectiveness of the methodology.

There are still many unanswered questions concerning the impact of new microelectronic, integrated circuit, digital, microcircuit technology on EMC. This report represents the first steps taken to determine that impact and to establish a theoretical basis to provide the necessary technology to ensure EMC.

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PROGRAM DESCRIPTION

1.1 OBJECTIVE

EMC in Microelectronics comprises the definition and study portion of a long range program whose goal is to develop Electromagnetic Compatibility (EMC) analysis tools; i.e., analytical models, prediction capabilities, and design guidelines for air, space, and ground systems or subsystems containing microelectronics. As a primary objective, this program is to develop and implement a methodology for determining the impact of the Electromagnetic Environment (EME) in systems employing microelectronics. In so doing, the program will identify deficiencies, technological and otherwise, that may limit application of the methodology.

This report describes the results of the study including the definition of the performance criteria, the development of the methodology, and a sample implementation to illustrate its application.

1.2 BACKGROUND

The thrust into the Electromagnetic Compatibility area was stimulated by the new integrated circuit technologies scheduled for inclusion in USAF equipments and systems in the mid 1980s. Questions arising as to the EMC technology impact on overall system performance, standard electromagnetic compatibility tests, analysis procedures and models, etc., were unanswered. The Rome Air Development Center (RADC) determined that only fragmented information was available within the EMC community. In addition, efforts up until this time addressed only portions of the total EMC problem.

A general approach to EMC in systems or subsystems containing microelectronics was sought. In formulating this approach, it was necessary to examine the applicability of work performed by other technical communities, such as reliability and electromagnetic pulse (EMP). Because the information necessary to complete this effort is fragmented, partitioned and overlaps several disciplines, a structured approach (methodology) was chosen by RADC to answer questions about EMC in microelectronics.

1.3 PROGRAM OUTLINE

The overall program for determining the impact of EMC in microelectronics is comprised of three major elements:

- 1. <u>Definition</u> Development of EMC performance criteria: defining adequate operation of microelectronic systems or subsystems in an EME.
- 2. Methodology Establishment of a step-by-step procedure for assessing EMC in microelectronics and applying the performance criteria.
- 3. <u>Implementation</u> Application of the methodology to a typical system to assess the effectiveness of the methodology.

This report details work accomplished during each of the program elements.

SECTION 2

THE EMC PERFORMANCE CRITERIA

2.1 BACKGROUND

In general, electromagnetic interference control for military electronic equipments centers on compliance with MIL-STD-461, in effect since 31 July 1967 as a triservice standard. It sets forth limits for both electromagnetic emissions and susceptibilities. Those familiar with such standards recognize many elements of MIL-STD-826A within it which predates MIL-STD-461 by a little over three years (30 June 1964). Many of the basic concepts are seen in even earlier specifications, such as MIL-I-6181D, (25 November 1959) and MIL-I-26600, (2 June 1958).

All of these standards and specifications are based on a deterministic concept; i.e., the assumption that one can determine the EMC characteristics of any equipment to any desired accuracy, and that the characteristics of the population can be determined by any one sample. The concept of compatibility has evolved as if these deterministic laws could specify all future conditions as long as sufficiently accurate information could be obtained.

Deterministic criteria are adequate as long as the measured or calculated parameters accurately predict performance. Whenever uncertainties in what is being measured exceed the accuracies necessary for correct prediction, other measures are required.

2.2 THE PROBABILISTIC NATURE OF EMC

For the analog and simple digital equipments of the 1950s and 1960s, the use of deterministic criteria was considered cost effective given the minimal availability of modeling and prediction capabilities during that time. Since analog devices degrade in a linear or near linear fashion with increasing interference, low-level degradation can often be seen in a given output before the output performance degrades beyond tolerance. Such a response allows for the inaccuracy that a deterministic criterion inherently causes.

Unlike most analog devices, digital components and therefore, digital based equipment exhibit nonlinear responses to interference. Instead of graceful degradation with increasing interference levels, digital equipment may suffer abrupt degradation with relatively small increases in interference over a given level.

If one considers the interfering signal to be a change in dc bias at the input to a logic gate due to the EME, it can be shown that the response of "identical" components will vary from individual component to component.^{2,3} Manufacturers only guarantee the maximum dc voltage at which their device will recognize an input as a "low", or the minimum at which it will recognize a "high".

For example, in a CMOS B-series digital IC, the maximum dc voltage at which the device is guaranteed to recognize the input as a "low" is 1.05 volts; and the minimum value for a guaranteed "high" is 3.95 volts. Although the manufacturer does not guarantee the device response between these levels, the device output will be recognized by subsequent devices as either high or low.

If one were to test N devices at a given input voltage to determine now many recognized that input as high, a distribution may result as shown in figure 2-1. Normalization by N, as N increases, will approximate a probability function (see figure 2-2) for the voltage at which the device senses a "high" input. Such curves demonstrate the response within the "undefined" region of logic devices. For example: a device is chosen at random from the group defining figure 2-2. This device is tested with an interference signal inducing 2.0 volts on the input. Because of its response characteristics, this particular device happens to respond with a "correct" low. A deterministic approach would define all such devices as compatible given that particular interference level. In reality, figure 2-2 shows that the probability of sensing an input as an incorrect high is actually 0.25. In the long run, one out of every four devices would be incompatible given that same interfering signal.

Variation in device response is only one parameter which must be considered if accurate prediction of system operation in a given environment is required. Electromagnetic Interference (EMI) data, particularly that of unintentional emitters and receptors, is largely the result of testing performed to such standards as MIL-STD-462. These measured results, however, are greatly influenced by elements beyond test operator control. Radiated emission measurements can be subject to variations of as much as ±40 dB. Above the shield room resonant frequencies, these variations are primarily due to standing waves in the shielded enclosures. At lower frequencies, coupling nulls may result from near field effects.4,5,6 In the frequency range of 14 kHz - 30 MHz, where rod antennas are used, levels may vary due to capacitive coupling effects between the antenna and nearby objects not directly associated with the test.

Emission levels may also vary due to minor differences in assembly of the unit under test. One of the authors of this report measured a 20 dB difference between supposedly identical production units. This was traced to differences in the length of a single ground wire. Variations of up to 40 dB have been measured in coupling between adjacent shielded wires due to differences in length of the shield pigtail. Other variations could be expected due to mechanical factors such as screw torque, paint masking, or cable bundling.

Each factor contributes to variability in measurements, and during any one EMI test, each combines with other factors to produce one particular result. Treating this result in a deterministic manner ignores the probabilistic nature of all factors contributing to that particular outcome.

These variations were depicted in a series of experiments described by J. Roe. 8 Figure 2-3 shows his results of the measured probability that a charge amplifier would exceed a given threshold (probability of upset) for a typical MIL-STD-461, RS03 test. One hundred independent samples of the device's response were taken at each power level, and the probability of upset was calculated by dividing the number of times the unit exceeded the specification by the sample size. Note that the probability curve approximates a Gaussian distribution and that the incident power levels of upset ranges from less than 10^{-5} watts to 10^{-3} watts, more than 20.0 dB.

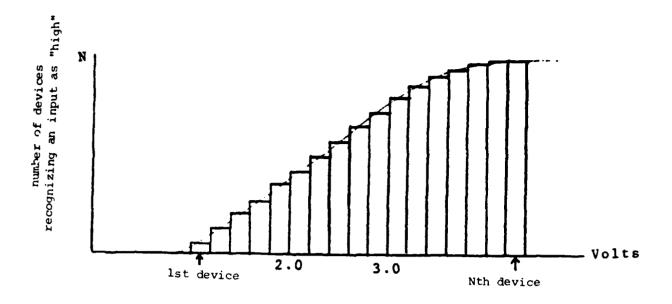


Figure 2-1. Cumulative Sampling for Number of Devices Recognizing an Input as "High"

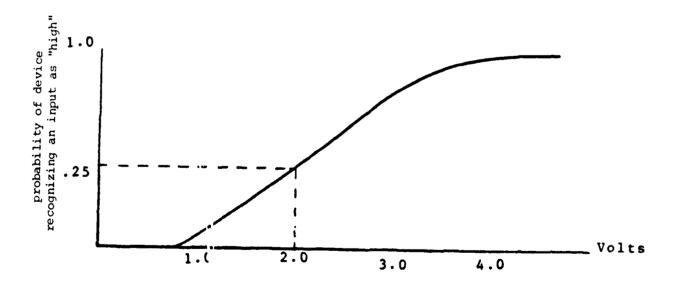
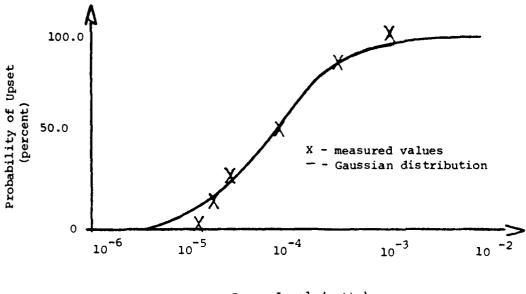


Figure 2-2. Cumularive Probability Function for the Number of Devices Recognizing an Input as "High"



Power Level (watts)

Figure 2-3. Results of Statistical Analysis on a Charge Amplifier⁸

Safety margins are widely used by the EMC community to account for inadequacies in measurement or prediction. MIL-E-6051D, Electromagnetic Compatibility Requirements, Systems, for example, suggests a minimum of 6 dB for a safety margin (20 dB when electroexplosive devices are involved) for some equipment categories. The use of safety margins as a general rule in system compatibility design is questionable unless the actual bounds are well known and appropriately factored into the margin. As previously mentioned, plus or minus 40 dB variations exist in radiated emission measurements alone. 4,5,6 Assuming a worst case variation of 40 db in both emissions and susceptibility an 80 dB safety margin is suggested although such a margin would likely result in gross over design. Yet, a lesser margin could result in incompatibility. A more realistic approach is to recognize the probabilistic nature of EMC and to address it on a sound statistical basis.

2.3 THE PROBABILISTIC APPROACH

Reliability Engineering has dealt with probabilistic criteria for a number of years. Reliability is defined on that basis as "... the probability that [an equipment]... will not fail to operate satisfactorily in a given time interval ...".9 In reliability analysis it is not possible to predict when a specific component will fail. It is only necessary to know as a class, either the Mean-Time-Between-Failure of the component (M) (or its reciprocal, λ , defined as the failure rate), or the mean life and its standard deviation. From this, one can predict overall reliability for systems comprising thousands of components and verify the prediction through testing,

Digital equipment complexities have reached a level wherein the probabilistic nature of the events can no longer be ignored. Whether or not it is universally recognized, EMC is best defined in terms of the probability that a system will operate satisfactorily in a given electromagnetic environment.

2.4 THE COMPATIBILITY FACTOR

As discussed in paragraph 2.2, the electromagnetically induced upset problem involves many variable conditions which combine to produce the overall effect. The probabilistic approach requires a parametric model for these variables and their mathematical combination, to yield a single "factor" that defines component performance in a specific environment as a probability. Thus, the compatibility factor derived in this section is a probabilistic "figure of merit". It is specifically defined as the probability that a component will operate satisfactorily in a specific electromagnetic environment over its entire range of desired signals. Definitions of terms relevant to this development are given in appendix 3 of this report.

2.4.1 UNDERSTANDING COMPONENT RESPONSE TO EMI

The first step for arriving at a compatibility factor is to understand component response. Generally, one defines component operation in terms of some performance criterion (PC). Examples of PC might be errors per second, articulation index, or any other measure of the satisfactory/unsatisfactory performance of the component.

Component response is defined if one can determine its operation as a function of interfering signal (i) and desired signal (s). Interfering signal refers to the level of EMI coupled into the component. Its units vary depending upon the component and coupling mechanism. If the component were an antenna, (i) might be expressed in volts/meter or received power (watts). For a data line, a more convenient unit for (i) might be current (amperes). The desired signal is important if the device response for a given interference changes over its range of normal operating signals. This effect is most evident in digital equipment, where device input and output impedances vary greatly for different inputs. Table I shows this input relationship for a typical two input NAND gate, where the desired signals are 0.0 and 5.0 volts. Note how impedances vary as a result of different combinations of the desired signal. Such variations greatly effect the EMI coupling mechanism.

Table I. Effects of the Desired Signal on NAND Gate DC Impedances

DESIRED S	SIGNAL			
Input 1	Input 2	Output	Impedance	Input Impedance, Input 1
0.0 V	0.0 V	15	ohms	8.6 kohms
0.0 V	5.0 V	15	ohms	8.6 kohms
5.0 V	0.0 V	15	ohms	1 Megohm
5.0 V	5.0 V	39	ohms	1 Megohm

In general, a <u>Performance Curve</u> (PC) results in the form given in figure 2-4. For such a curve, the PC is plotted versus the value of some function, (h), of the desired signal (s) and the interfering level (i). This function [h(s,i)] relates all relevant parameters to a single variable along the abscissa. For example, if

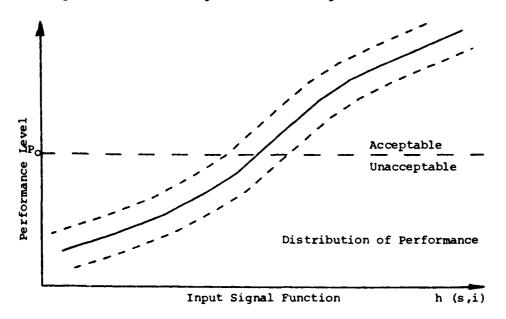


Figure 2-4. General Performance Curve

the desired signal is expressed as signal power and the interfering signal by received noise power, a convenient relationship is:

$$h(s,i) = 10 Log(s/i)$$
 (1)

which would give a signal to noise ratio in dB.

The last step in describing a component's response is to define the value of PC at some point along the ordinate axis, where operation is degraded such that any further degradation results in unsatisfactory performance; i.e., it is incompatible. This value, PC = Po, is defined as the minimum acceptable performance. It is represented as a horizontal line in figure 2-4.

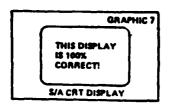
Figure 2-5 illustrates two examples of degraded operation. In the first instance, the bulb either works or does not. Minimum acceptable performance is easily defined. The second case illustrates displayed information lacking an exclamation point. From an operational standpoint it is unlikely that the missing exclamation point would significantly effect mission success. In this instance, defining Po as "no malfunction..." could add significantly to program cost without an actual increase in performance. A much better PC might be percent screen correct, and let Po = 90%. Under such a definition, the component in Case 2 operates satisfactorily (compatible).



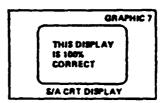


SYSTEM NOT WORKING-BULB BROKEN

CASE 1 SIMPLE SYSTEM



SYSTEM WORKING 100% ALL CHAR. CORRECT



SYSTEM WORKING 99.9% "!" MISSING

CASE 2 COMPLEX SYSTEM

Figure 2-5. What is Acceptable Performance?

2.4.2 MODELING COMPONENT VARIABILITY

From one "identical" component to the next there are variations in the performance curve, due to the inherent variability in components, as discussed in paragraph 2.2. This variability can be represented as an envelope around the original performance curve. If a component were picked at random from a population defined by this envelope, then its exact response could not be determined. Rather, response would be given in terms of a probability.

EMI performance curves do not exist for most equipments. The probabilistic concept may be addressed, however, by introducing a random variable, L, that defines equipment performance uncertainty. Specifically, L is defined as the minimum level of interference (denoted as ℓ) that causes unsatisfactory performance.

A start at probabilistically defining device response may be obtained by an experiment performed on a large population (N) of "identical" components. If the desired signal is held constant and the interference level is controlled, an approximate cumulative distribution for L arises by plotting the number of components exceeding Po versus interference level to upset. One assumes that if a component is incompatible at a level ℓ_1 , then it is incompatible for all higher levels $\ell > \ell_1$. The distribution increases with ℓ , up to some level, ℓ_{max} , where all N components fail. Finally, normalizing by N renders a cumulative Conditional Interference Function (CIF), represented as $F_L(\ell | S=s)$. An example CIF is given in figure 2-6.

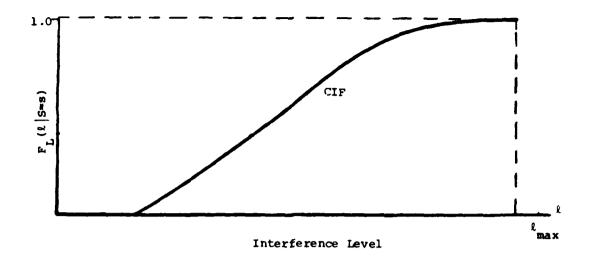


Figure 2-6. Effect of Component Variability

A Conditional Compatibility Function, (CCF) may then be defined simply as:

$$C(\ell|S=s) = 1.0 - F_L(\ell|S=s).$$
 (2)

This function is important because it is deduced from experimental data based upon component upset and gives the probability a component will operate satisfactorily.

Up until this point, a known interference level, (ℓ) has been assumed. Variations in interference levels also exist, as demonstrated in paragraph 2.2. Therefore, a random variable (I)*is defined that allows for variations in interfering level (ℓ). Its associated probability density function is [$f_I(i)$]. One can determine its probability distribution function as the probability of the interference being equal to or greater than a specific level ℓ ; i.e.,

$$P(i \geq \ell_1) = \int_{\ell_1}^{\infty} f_{I}(i) di.$$
 (3)

Given $f_{I}(i)$, the expected value of the CCF of component response over all possible values of interference for a given desired signal becomes;

$$C_{S}(s) = \int_{\ell_{1}}^{\infty} C(\ell | S=s) f_{I}(\ell) d\ell$$
 (4)

where $C_S(s)$ is called the <u>Expected Conditional Compatibility</u>. The values of $C_S(s)$ may be considered the compatibility factor of a component in a specific environment (defined by $f_I(\ell)$), at a given desired signal.

^(*) The random variable associated with the environment is described by (i). When this interference is defined at the component level, random variables (l) and (i) are synonymous. The remainder of this development uses only the random variable (l).

Finally, if the desired signal's density function, $f_S(s)$ is known, an all encompassing compatibility factor becomes:

$$C = \int_{-\infty}^{\infty} f_{S}(s) \left[\int_{-\infty}^{\infty} C(f|S=s) f_{I}(f) df \right] ds$$
 (5)

C therefore represents the average of the Compatibility Factors for all possible values of desired signal, weighted by the probability density of each possible value of desired signal.

Equations (4) and (5) provide the framework for calculating the compatibility factor of a component, based upon the statistical response of the component, and the density functions of interference and desired signals. The impact of such a figure of merit depends upon present and future technology's ability to determine these functions in a generic sense.

Earlier work in the EMC community^{4,8} indicates that one possible approximation to these functions might be the Gaussian distribution function. The following derivation assumes that the desired signal is a constant, and that the component response and interfering level functions can be approximated by a Gaussian density function. Using such assumptions, one can demonstrate how the earlier derivations are made applicable.

2.4.4 POSSIBLE APPLICATIONS

In this analysis, a compatibility factor is derived for the case where the CCF is Gaussian, and where desired signal is assumed constant, or

$$\mathbf{F_L}(\ell|\mathbf{S=s}) = \mathbf{F_L}(\ell) = \frac{1}{\sigma_L \sqrt{2\pi}} \int_{-\infty}^{\infty} e^{-(\ell - \mu_L)^2/2\sigma_L^2} d\ell$$
 (6)

where

 μ_L = the mean component response to interference and

 σ_{L} = its standard deviation.

A density function for $F_L(\ell \mid S=s)$ is defined by

$$\mathbf{f}_{\mathbf{L}}(\hat{\mathbf{x}}) = \underline{\mathbf{F}_{\mathbf{L}}(\hat{\mathbf{x}} \mid \mathbf{S} = \mathbf{s})}$$

where $f_L(\ell)$ is a Gaussian density function over the random variable L. Equation (4), which gives Expected Conditional Compatibility, may be rewritten as:

$$C_{S} = \int_{-\infty}^{\infty} f_{I} (i) \int_{0}^{\infty} f_{L} (l) dl i dl$$
 (8)

This relationship may be more easily evaluated by introducing another random variable [Y = L - I]. Note that, whenever $Y \ge 0$, the component incompatibility threshold exceeds the interfering level and the component will function (i.e., is compatible). The expected conditional compatibility is then the probability that $Y \ge 0$ for the combined density function:

$$C = \int_{0}^{\infty} f_{\mathbf{Y}}(\tau_{i}) d\tau$$
 (9)

Figure 2-7 demonstrates the function $f_Y(\eta)$ where η represents the differences in levels between L and I.

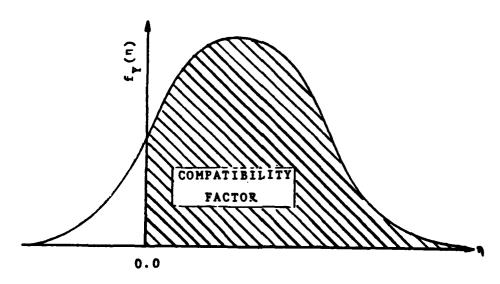


Figure 2-7. The Function $f_{Y}(\eta)$

When $f_L(\ell)$ and $f_I(i)$ are both Gaussian density functions, $\ f_Y(\ ^\eta)$ is also a normal density:

$$C = \int_{-\infty}^{\infty} f_{Y}(\eta) d\eta = \frac{1}{\sigma_{Y}\sqrt{2\pi}} \int_{0}^{\infty} e^{-(\eta - \mu_{Y})^{2}/2\sigma_{Y}^{2}} d\eta$$
 (10)

where

$$\mu_{\mathbf{Y}} = \mu_{\mathbf{L}} + \mu_{\mathbf{T}} \tag{11}$$

and

$$\sigma_{\mathbf{Y}} = \sqrt{\sigma_{\mathbf{L}}^2 + \sigma_{\mathbf{T}}^2}.$$
 (12)

 $\mu_{\rm I}$ and $\mu_{\rm L}$ are the mean interfering level and mean device response. Symbols $\sigma_{\rm L}$ and $\sigma_{\rm I}$ are the standard deviations of device response and interference, respectively.

To change equation (10) into standard form we transform η into a new variable, Z, such that $Z\approx (\eta-\mu_Y)/\sigma_Y$

then

$$dZ = (d\eta)/(\sigma_Y)$$
 (13)

and for $\eta = 0$ (lower limit of integration of equation 10)

$$Z = (-\mu_{\mathbf{Y}})/(\sigma_{\mathbf{Y}}) \tag{14}$$

Substituting into equation (10) yields:

$$c = \frac{1}{\sqrt{2\pi}} \frac{\int_{-\mu_{Y}}^{\omega} e^{-z^{2}/2} dz$$
, (15)

letting

$$z_{o} = \frac{\mu_{\Upsilon}}{\sigma_{\Upsilon}} = \frac{\mu_{L} - \mu_{I}}{\sqrt{\sigma_{L}^{2} + \sigma_{I}^{2}}}, \qquad (16)$$

then

$$c = \sqrt{\frac{1}{2\pi}} \int_{Z_0}^{\infty} e^{-z^2/2} dz$$
. (17)

To evaluate C, tables of the error function may be used as follows:

$$C = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{Z_0} e^{-Z^2/2} dz = \frac{1}{2} + \frac{1}{\sqrt{2\pi}} \int_{0}^{Z_0} e^{-Z^2/2} dz$$

(18)

$$C = \frac{1}{2} + \operatorname{erf}(z_0) ,$$

where $erf(Z_0) = 1/(\sqrt{2\pi}) \int_0^{Z_0} e^{-Z^2/2} dZ$.

In this example it was shown that the probabilistic nature of EMC may be defined by a relationship between device response (L) and interference level (I), when both random variables are normally distributed (Gaussian). An expression for the probability of a component performing adequately in a given environment or compatibility factor (C) can be calculated by knowing only the means and standard deviations of the two random variables.

The relationship betwen μ_L , μ_I , σ_L , σ_I easily lends itself to tabularization of the compatibility. Rearranging equation 10 we can reduce to two variables in a and b:

$$z_{0} = \frac{\mu_{L} - \mu_{I}}{\sigma_{I} \sqrt{1 + (\sigma_{I}^{2})/(\sigma_{L}^{2})}}$$
(19)

or

$$z_0 = \sqrt{\frac{b}{1+a^2}}$$
 (20)

where
$$a = \sigma_I/\sigma_L$$
 (21)

$$\mathbf{b} = (\mu_{\mathbf{L}} - \mu_{\mathbf{I}})/\sigma_{\mathbf{L}} \tag{22}$$

Plotting equation (19) for particular values of $Z_{\rm O}$ (and thus specific values of compatibility factor (C)) yields figure 2-8. Thus, compatibility factor can be reduced to a form of lookup table or graph, given the standard deviation, and mean of the interfering level and device response characteristics.

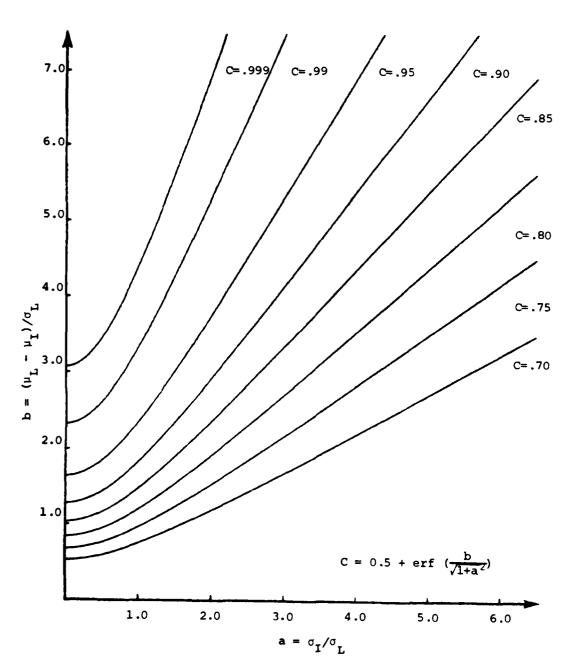


Figure 2-8. Graphical Solution Relating C to Means and Standard Deviations of L and I

SECTION 3

APPLYING PROBABILISTIC

PERFORMANCE CRITERIA - A METHODOLOGY

3.1 INTRODUCTION

In the previous section, a new approach to EMC performance criteria was presented in which the probability of successful operation in a given EME formed the basis for compatibility. Application of the probabilistic criteria, however, requires more than just establishing the limits. A method is needed by which these criteria may be applied to management, design, analysis, and testing at all levels.

Methods of dealing with statistical data have been developed in other disciplines, Reliability Engineering being perhaps the most closely related to EMC. The term compatibility factor was derived in a manner similar to reliability. It is not surprising then that several widely used tools of Reliability Engineering might be modified to fit EMC needs.

Note that the title of this section is \cdots <u>A</u> Methodology. A program which addresses a problem and solution with such far-reaching consequences cannot claim to have addressed all possible approaches and selected the single best one. One possible approach to applying probabilistic consideration to EMC performance is presented.

3.2 REQUIREMENTS

The requirements for a methodology to digital system EMC control indicated a need for one which allowed access by any group in the equipment procurement/design/installation cycle.

Application at the systems level benefits a Program Office in developing EMC performance specifications. At this level, the compatibility factor and EME must be decided and specified. The Program Office must also have the tools to develop these requirements from the known factors of mission profile, system importance to mission success, and/or platform/crew safety.

The Systems Engineer, given the requirements for compatibility factor, allowable error rate, and EME, must be able to allocate the compatibility factor to the various sublevels in a manner that realizes the most cost effective compliance. The Systems Engineer must be able to determine critical functions, make quantitative tradeoff analysis, and track development while comparing predicted performance against requirements.

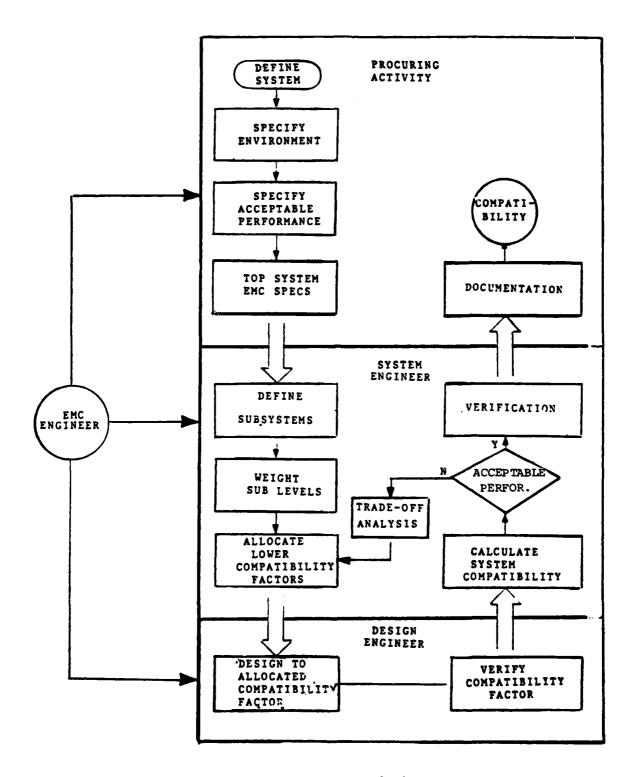


Figure 3-1. EMC Control Diagram

Given the compatibility factor and EME requirements by the Systems Engineer, the Design Engineer must efficiently determine critical circuits, components, interconnections, and the effects of EME on the design.

Generally, the Program Office is interested in examining the system from the top-down; i.e., from a high level to lower levels, and the Design Engineer is interested in a bottom-up approach whereby the effects of EME at the circuit levels are traced upward. The Systems Engineer may require either or both approaches in determining optimal design. Because of these requirements, a bidirectional approach was developed into the methodology which allows entrance into and control at any stage of the development cycle. This concept is demonstrated in figure 3-1.

3.3 AN OUTPUT CLASSIFICATION INDEX - DETERMINING THE OVERALL SYSTEM COMPATIBILITY FACTOR

In the previous section, the compatibility factor was defined and derived. This paragraph presents a method by which the numerical value for the compatibility factor may be assigned to system outputs based upon the effect a particular output has to system operation (severity) and the importance of that system to mission performance (priority).

Severity (S) is defined as a numerical value associated with the effect of an output upset on system/subsystem/assembly performance. In general, severity is a function of several parameters, $\mathbf{s_i}$, that can be used to define the output conditions, such that

$$S = A(s_1, s_2, s_3, ..., s_m),$$
 (23)

where the function A = "output classification index" (OCI).

Priority is defined as the importance of the entire system under consideration to the mission in its intended environment. The value for priority (P) ranges from P_{\min} , for a system of minimal importance to the mission performance to P_{\max} for a system of maximum importance. Compatibility factors may then be assigned as

$$C = g(S, P) \tag{24}$$

where g is some function of severity and priority.

The function g is bounded by C_{max} , the highest practical compatibility factor, considered by examining both the theoretical limit on C and the cost to achieve it. The definitions of S and P require that

$$C_{\max} = g(S_{\max}, P_{\max}). \tag{25}$$

The remainder of this section quantifies the above relationships by giving a possible assignment procedure. Although the actual numbers are not verified, the parameters for severity discussed are seen as the major contributors to the output classification index.

3.3.1 AN EXAMPLE OUTPUT CLASSIFICATION INDEX

Four parameters can seen to govern the assignment of severity:

- Output function effect
- redundancy
- recoverability and
- output control.

Output function effect refers to the degree of loss of system function created by an output upset. Assessment can be arbitrary or specified as in MIL-STD-1629 (SHIPS). These assessments may be given such names as Catastrophic, Critical, Major, Minor etc., depending on the effect of the upset to mission performance and/or platform/crew safety. As an example these are defined as follows (patterned after those of MIL-STD-1629 (SHIPS)):

- Catastrophic An upset which may cause death or weapons systems loss;
 e.g., inadvertent triggering of self destruct or launch of missile.
- <u>Critical</u> An upset which may cause severe injury, major property damage, or major system malfunction which will result in system degradation; e.g., loss of ELINT system functioning.
- Major An upset which may cause minor injury, minor property damage or minor system malfunction which will result in delay or loss of availablity of a system e.g., degradation of self test function.
- Minor An upset not serious enough to cause injury, property damage, or system damage, but could result in annoyance; e.g., intermittent error in display.

Another possible assessment criterion is the percent performance degradation as shown in Table II. Thus, output function effect may be determined either qualitatively or quantitatively.

Output Function Effect	Percent Disabling	Numerical Quantization
Catastrophic	90 - 100	4
Critical	75 - 90) 3
Major	20 - 75	2
Minor	<20	1

Table II. Output Function Effect Quantization

The remaining three severity parameters combine in a simple manner and classify the output. Redundancy refers to possible backup systems to the system in question. Recoverability refers to the possibility of restoring the system to normal operation after upset occurs. Output control refers to how an output is acted upon. It may be controlled manually or automatically. Automatic control removes an override option and thus increases severity whereas manual control allows a degree of decision that decreases severity.

Figure 3-2 shows a manner in which the three parameters may combine to determine output classification. Considering each separately, a value of 1 or 0 is assigned to it depending on whether or not it increases severity. The values are then summed. Adding 1 to the sum gives a number ranging from 1 to 4 which defines output classification. For example, if an output is non-redundant, recoverable, and automatic control the output classification equals:

oc = 3

Given output function effect and output classification, the severity may then be read off the output classification index given in figure 3-3. The relationship chosen arbitrarily between the ith row and jth column and severity is:

$$S = [(J-1) + (I-1)]/6.$$
 (26)

Severity therefore, is chosen to range between 0.0 to 1.0. For example, an output classification of 3 and an output function effect of 4 translates to a severity of .83 out of a possible 1.0.

Severity can be used at two levels of analysis, for determining top system compatibility or in a bottom-up technique, EMECA, covered in Section 3.5. The remainder of this section demonstrates the use of severity for system compatibility specification.

3.3.2 SPECIFYING TOP COMPATIBILITY FACTORS

As stated in this section's introduction, severity of an output upset is not the only condition needed to specify top compatibility factors. One must also consider the importance of that system to its intended mission or priority. Priority is based upon the procuring activity's judgement as to the importance of the system to mission performance. Note that there is a subtle difference between output function effect and priority. The former refers to how an upset affects the system performance while the latter is concerned with how the system effects mission performance.

Priority may be quantized to any number of levels. For simplicity, this example chooses four levels of priority, P, ranging from top priority (4) to low priority (1). For instance, top priority (4) infers that system loss would be irreversibly damaging to the mission. Low priority (1) means that system loss in no way threatens mission performance.

The conventions used by this example are that the higher the numbers for severity or priority, the greater the need for a high probability of compatibility. Thus, equation 24, which relates severity and priority to compatibility factor, is chosen so that as severity and priority increase, so does the assigned value of C. If the product of S and F is used, one has a relationship that increases as either S or P increases. However, a problem arises in that:

$$g_{\text{max}} (S,P) = S_{\text{max}} \times P_{\text{max}} = 1.0 \times 4 = 4$$
 (27)

and the theoretical maximum of C is 1 (although the practical limit for C_{max} may only approach 1.0).

1. REDUNDANT
$$\longrightarrow$$
 $I_1 = 0$
NON REDUNDANT $I_1 = 1$

2. RECOVERABLE \longrightarrow $I_2 = 0$
NON RECOVERABLE \longrightarrow $I_2 = 1$

3. MANUAL CONTROL \longrightarrow $I_3 = 0$
AUTOMATIC CONTROL \longrightarrow $I_3 = 1$
OUTPUT CLASSIFICATION = $1 + I_1 + I_2 + I_3$

Figure 3-2. Determining Output Classification

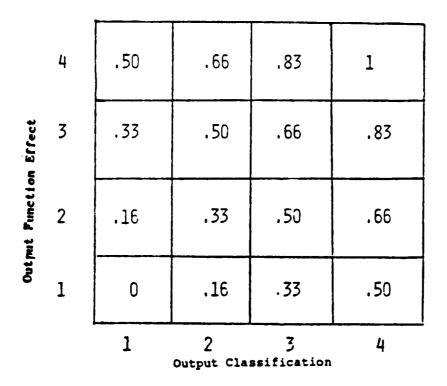


Figure 3-3. The Output Classification Index

Therefore, some normalizing function is chosen to maintain C within its practical bounds. One possible technique is to use the product of S and P in a function whose output ranges from 0 to \leq 1. The error function erf(K) is a probabilistic function that relates K to a probability. As K gets large (greater than 1.0) erf(K) approaches 0.5. One may form the following relationship:

$$C = 1/2 + erf(K) \tag{28}$$

where $K = S \times P$. Such an equation is well tailored to the problems shown earlier. Table III shows some values of erf(K) and C, given $S \times P = K$.

Table III - The Relationship Between K and Compatibility Factor

<u>K</u>	erf(K)	Compatibility Factor
1	.341	.841
2	•477	•977
3	•498	•998
4	•4997	.99997

Thus, the maximum assignable C is:

$$C_{\text{max}} = 1/2 + \text{erf} (S_{\text{max}} \times P_{\text{max}}),$$

$$C_{max} = 1/2 + erf (4),$$

$$c_{max} = .99997.$$

The mimimum assignable C is

$$C_{\min} = 1/2 + erf(0.0)$$

$$c_{\min} = 0.5.$$

Figure 3-4 represents equation (28) graphically. Given any combination of severity (S) and priority (P) one may specify, for any output, the necessary compatibility factor.

In summary, the process of specifying compatibility factors for various system outputs involves three steps:

- 1. The determination of severity wing OCI,
- 2. the setting of system priority to procuring level, and
- 3. the calculation of assigned compatibility factor using g(severity, priority).

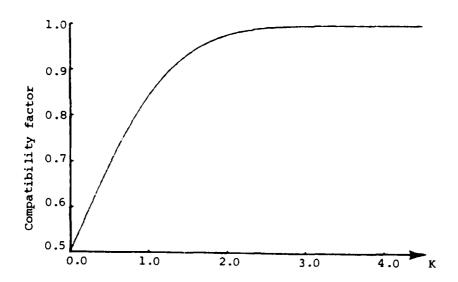


Figure 3-4. The Assignments of Compatibility Factor, given $K = (Severity) \times (Priority)$

Although preliminary at this time, the three step procedure is considered a good starting point for the process of assigning a compatibility factor.

3.4 FAULT TREE ANALYSIS

Fault Tree Analysis (FTA) was developed by Bell Telephone Laboratories in 1961 as a technique for performing safety evaluations of the Minuteman Launch Control System. 11 Since then, it has seen widespread and increasing usage in nuclear power plant design, chemical plant design, and in reliability determination. It is a top-down technique used to identify all possible fault conditions within a system which could lead to an undesired system condition. The Fault Tree itself is a Boolean Logic representation associated with the development of the top or basic fault. 12 Each possible event leading to the top event is defined as having two states: an CTF state with a logical value of zero; and an ON state with a logical value of one. Typically, an undesired state is defined as an ON and a desired, as OFF.

The top of the FTA represents the undesired output. The analysis procedure examines a fault potential from this event downward to all possible courses. Logic diagram symbols are used for the representation, making it readily adaptable to computer analysis. Standard Fault Tree symbols are shown in figure 3-5.

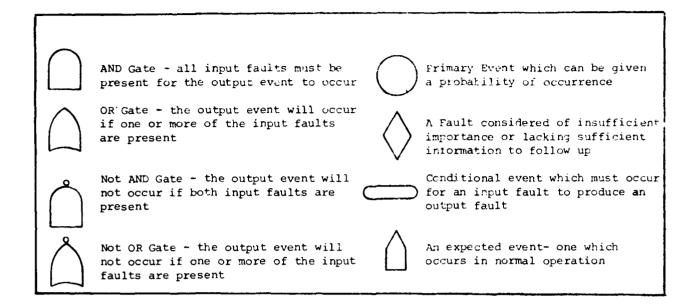


Figure 3-5. Standard Fault Tree Symbols

Probabilities are readily calculated using the Fault Tree. If the probability of each event is known or is specified, the probability of any higher event can be calculated using standard Boolean algebra. It is important to note at this point that statistical independence is assumed. As is often the condition, an interfering signal can be coupled into a circuit at more than one point. For purposes of this discussion, we will assume this is not true. In an AND gate, the probability of an output event P(0) is the product of the probability of each input event:

$$P(0) = P(A) \cdot P(B) \tag{29}$$

In an OR gate, the probability is of the form:

$$P(0) = P(A) + P(B) - P(A) \cdot P(B)$$
 (30)

For those cases in which P(A) and P(B) are below 0.1, the OR gate formula can be reduced to:

$$P(0) = P(A) + P(B)$$
(31)

For example, consider that P(A) = 0.01 and P(B) = 0.001. If A and B are combined in an AND gate (figure 3-6), then both events A and B must occur in order for an output to occur.

On the other hand, if A and B are combined in an OR gate, as in figure 3-7, then the output occurs if either event A or B occurs.

$$P (0) = P (A) \cdot P (B)$$

$$= (0.01) \cdot (0.001)$$

$$P (0) = 0.00001 = \frac{1}{100.000}$$

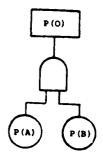


Figure 3-6. Probability Through an AND Gate

$$P(0) = P(A) + P(B)$$

$$P(0) = (0.01) + (0.001)$$

$$P(0) = 0.011 = \frac{11}{1000}$$

Figure 3-7. Probability Through an OR Gate

A more detailed description of FTA is found in the literature references, 11, 12, 13, 14, 15, 16, 17, 18, 19.

The complexities of FTA expand geometrically as the faults are traced downward. In typical systems, computer analysis techniques are necessary if the FTA is pursued beyond three levels (e.g., from system down to subsystem to assemblies). Such computer programs are already available and codes such as FTAP and IMPORTANCE^{20,21} developed for use by the military, appear applicable to EMC Fault Trees.

The principal application of Fault Trees is seen at Procurement or System Engineering level (although it can be used at any level). Its use at these levels is seen as a method of:

- Allocating Compatibility Factor requirements using Relative importance "weight" of various elements of a system.
- Computing the overall system integrated compatibility, given sublevel compatibilities.
- Tradeoff analysis of cost versus performance requirements using statistical importance.

3.4.1 APPLYING FTA

The following development demonstrates techniques already in use in Safety and Reliability engineering for the mathematical analysis of Fault Trees. The examples given are all easily done by hand. For large scale systems, computer codes such as FTAP and IMPORTANCE exist. These codes were developed by Lawrence Livermore Laboratories, partially under Air Force funding. This example analysis is intended to serve as a background to the mathematical basis of such computer codes.

3.4.2 DESCRIPTION OF CUT SETS

Preliminary to any application of the FTA is the determination of <u>cut sets</u>. A <u>cut set</u> is defined as the smallest set of primary events which must occur in order for the TOP event to occur¹². A <u>minimal cut set</u>, being a subset of the cut sets in which all redundant events are removed, is defined as the set of the combination of primary events whose presence cause the occurrences of the main event. Much work has been done¹⁴, ¹⁹ on methods for obtaining cut sets. Here a simple example is used to illustrate cut set derivation.

Figure 3-8 shows a simple Fault Tree of four primary events (labeled A to D), and six gates (numbered 1 to 6). Using Boolean algebra, a mathematical expression for the top event may be derived from figure 3-8 as follows:

Gate 6 has input C, B ANDed together. This may be written as:

$$X_{5} = CB \tag{32}$$

Gate 5 has the output of gate 6 (X5) and A ORed together:

$$X_4 = A + X_5$$

$$X_4 = A + CB \tag{33}$$

Gate 4 has inputs of C, B ORed together:

$$X_3 = C + B. \tag{34}$$

In a similar fashion, the outputs of gates 2 and 3 $(X_1 \text{ and } X_2)$ are:

$$X_1 = A (C + B) \tag{35}$$

 $X_2 = D (A + CB)$

Finally, the TOP event is the ORing of X_1 , X_2 :

$$TOP = A (C + B) + D (A + CB)$$

Reducing:

$$TOP = AC + AB + AD + BCD$$
 (36)

The combinations AC, AB, AD, and BCD are the minimum cut sets of the original fault tree. The relationship between cut sets, primary events, and top fault is given by equation (36), and may be represented graphically as shown in figure 3-9. The effect of cut set analysis, then, is that any general fault tree construct may be rewritten into a "standard" fault tree. The implication is that, in order for any top event to occur, at least one cut set must occur. For a cut set to occur, all the elements comprising it must occur simultaneously. Therefore, a cut set acts as an ANDing of all its elements and all cut sets can be ORed to determine top fault.

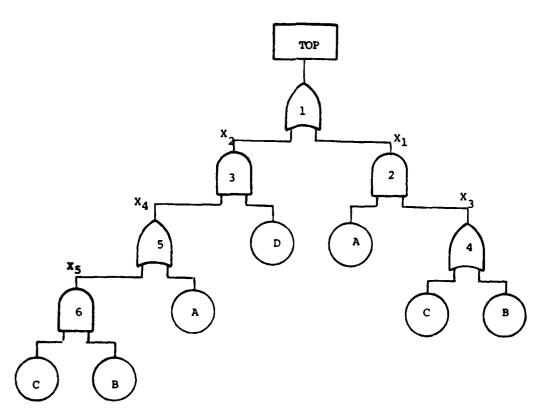


Figure 3-8. Example of a Fault Tree

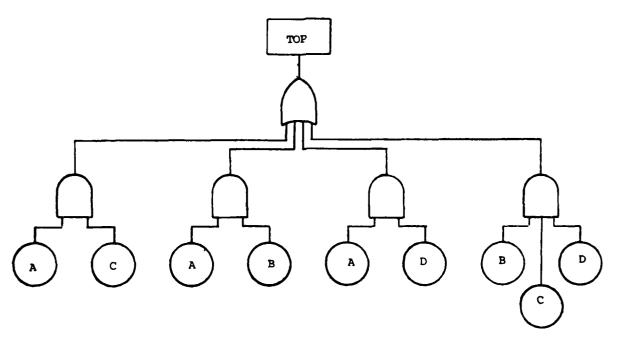


Figure 3-9. Graphical Representation of Cut Sets

Many techniques exist for calculating minimum cut sets, ranging from Boolean algebra or inspection for simple trees to computer codes (FTAP) for complex systems. Detailed explanation of these methods is beyond the scope of this study and the interested reader is referred to a text for further information²².

3.4.3 COMPATIBILITY FACTOR ALLOCATION

Given the minimum cut sets of a fault tree, one has all the information necessary for determining the structural importance of every primary event, or weight. In a system analysis, primary events generally refer to low level faults; e.g., assembly, subassembly. Thus, one has a ready tool for allocating lower level compatibility factors based upon how that low level fault is related to the system. The first step in the allocation process is to mathematically determine these primary fault weights.

Weight is calculated by determining how many cut sets contain a primary fault and the rank of each of those cut sets. The rank of a cut set refers to how many elements it contains. The difference between cut sets of two and three primary events is that the former needs only two simultaneous primary faults to cause top fault while the latter requires three. Thus, a 2-element cut set has a higher effect on top fault than a 3-element cut set. Mathematically, the Rank of the $k^{\rm th}$ cut set, X_k , is the reciprocal of the total number of primary faults (N) raised to the power of the number of elements n_k :

$$x_k = (1/N)^{n_k} \tag{37}$$

The next step is to calculate the actual weight of each primary event, (i). This is done by summing the ranking, (X_k) , of all cut sets k having i as its element and dividing by the total sum (X_i) . This can be represented as:

$$W_{i} = \sum_{i=1}^{m} X_{ki} / \sum_{i=1}^{m} X_{i}$$
(38)

where:

 m_{k} = number of cut sets which contain primary event, (i)

 x_{ki} = rank of cut set k, which contains primary event, (i)

m = total number of cut sets

The earlier example given in figure 3-9 demonstrates the process. Table IV lists the cut sets and calculation of the rank of each cut set. In this example N = 4, so for 2-element cut sets $X_i = 1/4 \times 1/4$, and 3-element cut sets $X_i = 1/4 \times 1/4$.

Table IV. Calculation of Cut Set Rank

Cut Set (K)	Contains Events	xi
1	A,B	1/16 = .06250
2	A,B	1/16 = .06250
3	A,D	1/16 = .06250
4	B,C,D	1/64 = .01563
		$X_{T} = .20313$

The weight is then calculated using Table IV. Primary event A is an element of cut sets 1, 2 and 3. Therefore,

$$W_A = (x_1 + x_2 + x_3)/x_T$$

 $W_A = (0.0625 + 0.0625 + 0.0625)/0.20313$

 $W_A = 0.92305$

Similarly, Primary Event B is an element of cut sets 2 and 4. Its weight becomes:

$$W_B = (x_2 + x_4)/x_T$$

 $W_B = (0.06250 + 0.01563)/(0.20313)$

 $W_B = 0.38463$

Table V summarizes the weight of each primary event. Special care should be taken in the design of elements directly responsible for primary fault A, as it has a much higher relative weight than the other primary events.

Table V. Primary Event Weights

Primary Event	Combination of Cut Sets	Relative Weight
A	1, 2, 3	0.92
В	4, 2	0.38
c	1, 4	0.38
D	3, 4	0.38

The last step in the process is allocating the top system requirements to lower levels. This is an iterative process with no unique solution, as system equations [e.g., equation (36)] have many variables. Since compatibility factor is the probability of no fault, and the top event in a FTA is "system fault", the incompatibility of the system:

$$\vec{C} = 1 - C \tag{39}$$

becomes the top fault probability.

Referring to relative weight tables for primary events aids considerably in allocation. For example, the weights in Table V show that primary events B, C and D have equivalent structural importance to the top event probability. Event A requires the greatest compatibility factor, since it has the highest weight. Given this information, a system incompatibility equation can be written from equation (36):

$$C_{\text{top}} = AC + AB + AD + BDC$$

$$C_{\text{top}} = C_{A}C_{X} + C_{A}C_{X} + C_{A}C_{X} + C_{X}^{3}$$

$$Where C_{X} = C_{B} = C_{C} = C_{D}.$$
(40)

Equation (40) may now be used to solve for incompatibilities of A, B, C and D. Again, the solution is not unique, however, given that C_A must be much larger than C_B , C_C and C_D , some bound may be placed upon the problem.

As an example, let the top compatibility factor for the above Fault Tree be 0.85. Equation 40 becomes

1 - 0.85 =
$$\overline{C}_{A}\overline{C}_{X}$$
 + $\overline{C}_{A}\overline{C}_{X}$ + $\overline{C}_{A}\overline{C}_{X}$ + \overline{C}_{X}^{3} .

Rearranging,

$$0.15 = \overline{C}_A (3\overline{C}_X + (\overline{C}_X^3/\overline{C}_A))$$

At this point the engineer must choose a value for either C_A or C_X . Since C_A has the highest weight, we will arbitrarily choose $C_A = 0.9$. This leaves:

$$10\overline{C_X}^3 + 3\overline{C_X} = 1.50$$

$$\overline{C_X} = 0.35$$

$$C_Y = 0.65$$

So, one possible allocation would be

$$C_{A} = 0.90$$
 $C_{B} = 0.65$

$$C_C = 0.65$$

$$c_0 = 0.65$$
 .

If this is not satisfactory, another iteration using different values may be undertaken. Perhaps the values of $C_{\rm B}$, $C_{\rm C}$, and $C_{\rm D}$ could be adjusted, by manipulation of equation (36).

3.4.4 CALCULATING SYSTEM COMPATIBILITY

Once allocation has been accomplished, the system under consideration will be under the control of various design engineers. Design should be made, at least from an EMC stand point, to conform to the allocated compatibility factor (C) as discussed in the previous section.

The system compatibility factor is a function of the incompatibilities \overline{C} , of primary faults and how they combine in cut sets. Figure 3-10 demonstrates generally how the cut sets of a system are related to the top event (incompatibility). For m cut sets the top system compatibility, C, is calculated by:

$$C = 1 - \sum_{k=1}^{n} C_k$$
 (41)

where C_k is the incompatibility of cut set k. The value of C_k is the product of the incompatibilities of all primary events contained in cut set k or:

$$\overline{C}_{k} = \prod_{i=1}^{m_{k}} C_{ki}$$
(42)

where C_{ki} = incompatibility of primary event i, contained in cut set k, and m_k = number of primary events in cut set k.

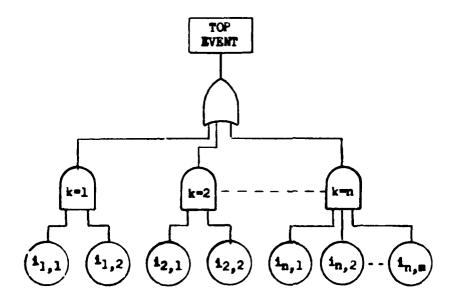


Figure 3-10. General Cut Set Relationship to Top Incompatibility

Now let us assume that in actual practice, the following compatibility factors have been determined for the example given in Figure 3-8.

$$C_A = .9$$

$$C_B = .75$$

$$c_{\rm C} = .6$$

$$c_D = .6$$

Note that C_A just meets its allocation (given on the bottom of page 28), C_B is higher, and both C_C and C_D are lower. We can now calculate the top system compatibility as follows:

The first step is to calculate the incompatibilities of the primary events and then apply these to each cut set:

$$\overline{C}_{\lambda} = 1 - 0.9 = 0.1$$

$$\overline{C}_{B} = 1 - 0.75 = 0.25$$

$$\overline{C_C} = 1 - 0.6 = 0.4$$

$$\overline{C}_D = 1 - 0.6 = 0.4$$

Cut sets 1 through 4 are listed in Table IV. The incompatibilities of the primary events of each are multiplied together to obtain:

$$\overline{C}_1 = \overline{C}_A \overline{C}_C = 0.04$$

$$\bar{C}_2 = \bar{C}_A \bar{C}_B = 0.025$$

$$\overline{c}_3 = \overline{c}_A \overline{c}_D = 0.04$$

$$\overline{c}_4 = \overline{c}_B \overline{c}_C \overline{c}_D = 0.04$$

The total system incompatibility is

$$\overline{C} = 0.04 + 0.025 + 0.04 + 0.04$$

$$\bar{C} = 0.145$$

yielding a system compatibility factor of

$$C = 1 - \overline{C}$$

$$C = 0.855$$

This compares favorably with the C = .85 which was the design goal.

3.4.5 TRADEOFF ANALYSIS - THE USE OF S-IMPORTANCE

If C is sufficient to meet specification, then the analysis is complete. A method is needed, however, in those instances where C is not adequate to meet system requirements. In such cases, the (statistical) importance of the primary events is useful.

The s-importance of primary event i (S_i) is defined as the "probability ...that i is contributing to top event failure, given the top event has failed." Fussell quantifies this expression in the following way:

- A = "at least one minimal cut set containing i is failed"
- B = "Primary Event i is failed"
- C = "Top event has failed"

Yk = "Cut set k containing i is failed"

m_i = number of cut sets containing i

Pr[X] = the probability of X.

Then by definition:

$$S_{i} = Pr[A \cap B | C]$$
 (43)

 $S_i = Pr[A]/Pr[C]$

$$s_i = Pr[Y_1UY_2U...Y_m]/Pr[C]$$

The incompatibility values for each cut set (calculated by equation (42)) can be applied directly to calculate the upper bound of s-importance by:

$$S_{i} \leq \left(\begin{array}{c} m_{i} \\ \Sigma C_{k} \end{array} \right) / C \tag{44}$$

The higher the s-importance of a primary fault, the more sensitive the overall compatibility is to change in that primary event. Thus, if a system is to be upgraded, the primary events having the highest s-importance should be addressed first. Higher compatibilities may be obtained with less change in the compatibilities of the primary event(s) with higher s-importance than in the compatibilities of lower primary events.

If the total system compatibility specification for the example on page 30 is increased from 0.85 to 0.90, then changes would have to be made to one or more of the primary event compatibilities to insure system integrated compatibility. Using s-importance, one can quantify decrease tradeoff analyses.

$$s_A = (c_1 + c_2 + c_3)/\overline{c}$$

= $(0.04 + 0.025 + 0.04)/0.145$

= 0.724

$$s_B = \frac{-}{(c_2 + c_3)/c}$$

= 0.448

 $S_C = 0.552$

 $s_D = 0.552$

From the above calculation, we note that event A most effects system change. Table VI lists the necessary changes in each primary event (given the other three do not differ) to change the system compatibility from 0.855 to 0.90. As indicated by the s-importances, event A requires the smallest upgrading to affect system change (43%), whereas event B requires 69% change and events C and D, 63%.

Table VI Trade-off Analysis Statistics

Primary Event	Initial Compatibility, Ci	Necessary Compatibility	Difference * (to upgrade)*
A	.9	.943	43%
В	•75	•923	69%
С	.6	•85	63%
D	.6	•85	63%

The engineer must then examine necessary upgrade versus cost to upgrade, as a tradeoff analysis. For example, although event A requires only a 43% improvement, the cost to obtain that change may be greater than the cost to change primary event D by 63%.

3.4.6 CONCLUSIONS ON FAULT TREE ANALYSES

This discussion is not intended to be an exhaustive study of the application of FTA to EMC. The ability to make meaningful Compatibility Factor assignments will determine the degree of usefulness of the method to the EMC Engineer. Further study will be required in this area to understand FTA, and to standardize EMC FTA construction and analysis, and to provide handbooks and training aids. The basic concepts of FTA, however, are viable and available for immediate application.

3.5 ELECTROMAGNETIC EFFECTS AND CRITICALITY ANALYSIS

The second half of the bidirectional approach, the Bottom-Up approach, is called the Electromagnetic Effects and Criticality Analysis (EMECA) which, along with its companion, The Electromagnetic Effects Analysis, is patterned after the Failure Mode Effects, Criticality Analysis (FMECA) of Reliability Engineering. Whereas the FMECA deals with a hard component failure and its effect on higher level performance, the EMECA and EMEA deal with "soft" failures or faults produced by electromagnetic interference pickup on wires, cables, component leads, circuit boards, etc. Ideally, all fault modes and combinations of fault modes would be considered, although multiple fault considerations could be expected to reach a complexity requiring computer manipulation. The difference between EMEA and EMECA is in the inclusion of the component compatibility factors in the EMECA, permitting analysis of the criticality of the signal path in question.

3.5.1 FMECA, A RELIABILITY TOOL

Compared with FTA, FMECA is a mature technology used by Reliability for a number of years. The basic FMECA format is tabular, usually in the format called out in MIL-STD-1629 (SHIPS) Procedures for Performing a Failure Mode, Effects and Criticality Analysis, or similar to that given by Gottfried in his 1973 Proceeding Product Liability Conference paper entitled "Quantitative Risk Analysis: FTA and FMECA".

(*) DIFFERENCE =
$$\frac{C - C_i}{1 - C_i} \times 100\%$$

FMECA and its close cousin Failure Modes and Effects Analysis (FMEA) are systematic approaches to identification and correction or compensation of failure modes in system design²³. They have been used for a number of years in critical space and missile systems.²⁴ Both of these standards as well as a handbook²⁵ have been published to direct their application.²³ Riefer²³ lists five major objectives for performing FMEA:

- To identify single point failure modes and define their effects.
- To identify those areas of a design where redundancy should be implemented.
- To identify compensating features where elimination is impractical.
- To identify redundancy which is not or can not be tested.
- To assist in ranking the most serious failure modes and for establishing a critical items list.

Similar requirements exist for EMC on circuitry consisting of digital microelectronics.

3.5.2 APPLYING THE EMECA

Although an EMECA may be applied at any level, it is primarily seen as a tool for use at the circuit design level. Like the FTA, complexity of the EMECA can be expected to increase geometrically as it is carried to levels further removed from the entry point. It is likely that its use will be confined to no more than three levels unless computer aided analysis is employed.

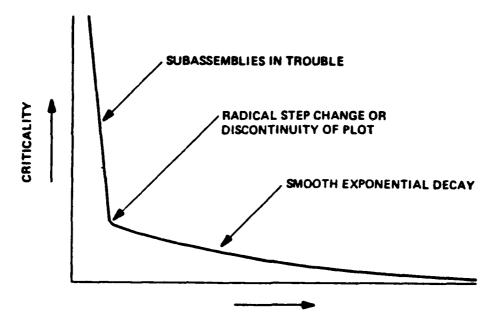
In the digital microelectronic application, the EMECA at the device level starts at a given component output (wire, bus, etch, etc.) and assumes that an EMI induced fault is present at that output. The effects of that fault on all subsequent devices are examined. In turn, the response is traced upward usually to an equipment output or other point where severity has been specified.

One standard by which severity may be specified is given in paragraph 3.3.1, utilizing the Output Classification Index. The implication is that if a lower level fault is sufficient to cause a high level fault of a known severity, then that lower level fault has an equivalent severity. In the case where low level fault (LLF) causes two or more high level faults (HLF) the LLF takes the value of the largest severity of the set of HLFs it causes.

Applying a severity analysis alone gives no consideration to the probability of the upset occurrence. Full consideration of component or low level equipment function under EMI introduces the term "criticality" and only such an analysis is termed EMECA.

The criticality of an upset is defined as the probability of its occurrence multiplied by the value of its severity. As earlier sections show, the probability of upset occurrence in a given electromagnetic environment is exactly the complement of the compatibility factor. Since the upset is defined at the output of a component, the complemented compatibility factor of that component times the severity of the output defines the criticality of the component:

By ranking all components with respect to criticality one will obtain a curve often demonstrated in Reliability analysis (figure 3-11). Addressing that curve, an EMC design engineer can maximize Compatibility design in much the same way a Reliability Engineer maximizes system Reliability. Specific EMC design tools, such as PC grounding layout, shielding and filtering can be applied to most critical areas in a cost effective and efficient manner.



SUBASSEMBLIES IN ORDER OF DECREASING CRITICALITY

Figure 3-11. Criticality vs. Number of Components

Application of the criticality equation, therefore, ties together the previously defined concepts of Severity and Compatibility. The EMECA is the complement to the system oriented Fault Tree Analysis. With the FMECA going from the bottom-up and the FTA from the top-down, one might expect that the two approaches would meet somewhere in the middle. Gottffried does report of "...one complex major system analyzed by two independent teams, one using FMEA and the other FTA,.... [having]...met in the middle quite nicely." 13

For the EMECA, where criticality is introduced, the initial step will still be the EMEA. From this point it is necessary to calculate pickup on the subsystem wiring from the EME to determine voltage levels at the devices. One of the IAP (Intrasystem Analysis) Codes such as GEMACS could be used for this determination. Next, the device response is determined from known (or measured) device characteristics. Then the EM environment characteristics are considered in order to yield component compatibility. Finally, the equation for criticality could be used and component criticalities compiled.

On very large systems it may be impractical to implement an EMECA at the component level. Reliability engineers often start FMECA analysis at the circuit level; one level above the component. A similar approach for the EMECA would pinpoint critical circuitry which could then be examined using the EMECA approach for detailed circuit design analysis.

SECTION 4

FLOW DIAGRAM

4.1 INTRODUCTION

In Sections 2 and 3 the concept of probabilistic performance criteria was introduced and various tools were described through which these criteria are applied to systems, subsystems, assemblies or even components. This section shows how these tools interact to obtain electromagnetic compatibility. The Flow Diagram in Section 3 is developed in more detail to show specifically where the various tools are applied throughout the design and development phases of a system.

4.2 THE IMPLEMENTATION FLOW DIAGRAM

The procurement of a system follows a progressive course from conception to installation and utilization. EMC control must be applied throughout. Implementation of EMC control is most effective, however, early in the procurement cycle, prior to installation. This methodology addresses these early activities:

- Procurement
- Systems Engineering
- Design Engineering.

Although in the following paragraphs, each activity is described as a separate entity, these functions may all be given to one EMC Engineer or distributed among many.

4.2.1 THE PROCURING ACTIVITY

The Procuring Activity is the funding organization of the system. It is responsible for taking the general mission requirements and formulating detailed performance specification. This is the level at which the EMC requirements are defined. As has been previously shown, these performance requirements must include:

- Compatibility Factor(s)
- Allowable Error Rate(s)
- Intended EME in terms of the expected means and standard deviations.

The Compatibility Factor is described in detail in Section 2. In order to standardize this requirement, a technique was presented called the Output Classification Index. This index permits the compatibility factor to be specified by defining Severity and Priority of the output. One point that must be emphasized is that it is not necessary or even suggested that the Compatibility Factor be specified for an entire system. A system may have many outputs each having a different Severity and Priority at various times during the mission. It is recommended that the Procuring Activity keep this in mind when developing the criteria. For example,

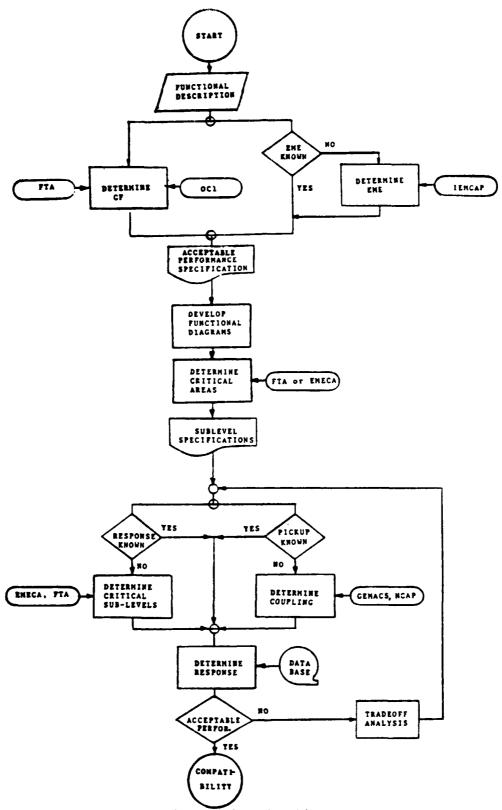


Figure 4-1. Flow Diagram

navigation radar would have a higher importance during flight than during takeoff and landing. The EME also would be expected to differ between these two points in the mission profile. Rather than require that all equipment meet all requirements at all EMEs, it would be advantageous to specify performance separately. In the radar example, one would expect a specification allowing a higher error rate with a lower Compatibility Factor for airbase related EMEs; and a higher Compatibility Factor with lower error rate during flight related EMEs.

Several approaches to specifying EMEs are possible. One approach is to use a modified IEMCAP code to provide the EME requirements in terms of mean peak powers (RMS equivalent peak), (voltages and currents for near-field) and standard deviations for all frequency ranges of concern. Another approach is to provide the data in tabular format similar to MIL-HDBK-235 for various mission scenarios. Here the determination of the EMEs at the system is left to the contractor. The former approach is more specific and easier for bidding purposes; the latter allows for greater possibilities of specification tailoring. With either approach, knowledge of the mean and standard deviations of the EMEs, most likely gathered through specific measurement programs, is required.

When several interrelated subsystems are separately procured, interaction among these must be considered. In these instances, a Fault Tree Analysis can be used to map the interactions and allocate the Integrated Compatibility Factors to the various subsystems as previously described in paragraph 3.4. Here other modified IAP codes, such as GEMACS, may prove beneficial in establishing inter-system EMEs.

4.2.2 SYSTEMS ENGINEERING

Systems Engineering functions as the organizing activity. Its responsibility is to configure the system, defining all subsystems and their interaction. Compatibility is addressed at the same time as system design begins and parallels the system engineering effort through implementation.

Early compatibility analysis involves taking procuring activity specifications and arriving at subsystem-assembly allocations. The Compatibility Factor allocation described earlier in this report uses a Fault Tree Analysis (intersystem) approach.

In many instances, the systems compatibility engineer may need to perform coupling analysis at various ports of the system to determine subsystem specifications. A GEMACS type analysis at the intersystem level can transform the procuring activity's EME into a form that the design engineer can utilize at the next level. Such analyses are necessary only at the systems engineer's discretion, based on system complexity, environmental levels and the overall system compatibility specification.

Once the above is accomplished, the focus of the compatibility analysis switches to the various design engineers. Attention swings back to the system engineer after design engineering is complete.

4.2.3 <u>DESIGN</u> ENGINEERING

The design engineer is responsible for the design, prototype and final construction of the component parts; i.e., circuits, subassemblies, assemblies. It is here that compatibility must be designed into the system. Meeting the compatibility

factor allocated to the assembly/sub-assembly is accomplished at this level. At this point in the design, bottom-up approaches such as the EMECA become very useful tools in describing weak links of an assembly.

Coupling analysis, such as XTALK or GEMACS, and modeling codes like NCAP or SPICE, can be used to provide insight into the components of an assembly that may cause incompatibility. At this level evaluation testing may be undertaken to obtain actual assembly Compatibility Factors and corrective measures can be most easily accomplished.

The variety of tools available at this level is much greater than at any other level. Finding the most effective tools and using them judiciously leads to efficient, cost effective design prior to system integration. If invested properly, the design phase can yield the greatest return in system compatibility.

As a final output, the design engineer uses testing and/or analysis to determine sub-level response and finally, compatibility factor. This effort is carried out simultaneously on all sub-levels and is fed back to systems engineering for evaluation and further action.

4.3 PUTTING IT ALL TOGETHER

Evaluation of sub-level design for compatibility takes place along the same lines as the allocation process with FTA. Using these processes the systems engineer can calculate overall system integrated compatibility as shown in paragraph 3.4.

If all sub-levels are designed within allocated specifications, theoretically, the compatibility design is completed. However, in cases where all specifications are not met, corrective action may be taken. Again, FTA can be used to determine the areas most likely to effect overall system compatibility by calculating s-importances. In any event, all redesign must be considered in light of cost and environmental parameters.

SECTION 5

IMPLEMENTATION EXAMPLE

5.1 INTRODUCTION

The purpose of the EMC in Microelectronics program is to define and develop a methodology for dealing with EMI phenomena relating to digital microcircuitry. The performance criterion was defined in the first portion of the program, and the previous sections introduced methods for implementing this criterion. In order to demonstrate the use of the criterion and methodology, as well as point out areas needing more study, an implementation has been performed on a simple ficticious system utilizing digital microelectronics. This report details the results of the implementation study.

5.2 SYSTEM DESCRIPTION

The system being used for the implementation is the Rod Control System (RCS) for a nuclear powered aircraft. The system is purely ficticious, and is not even particularly well designed, as will be seen later. The schematic of the RCS is shown in Figure 5-1.

The definition of the circuit, as it would be generated, is shown in three documents: the purchase specification and the environmental specification, generated at the procurement level and the hardware description package generated at the system/design engineering level.

5.2.1 PURCHASE SPECIFICATION

The purchase specification would consist of the functional requirements, the environmental specification and the output error criteria. Excerpts from this document might be as shown in Figure 5-2.

5.2.2 ENVIRONMENTAL SPECIFICATION

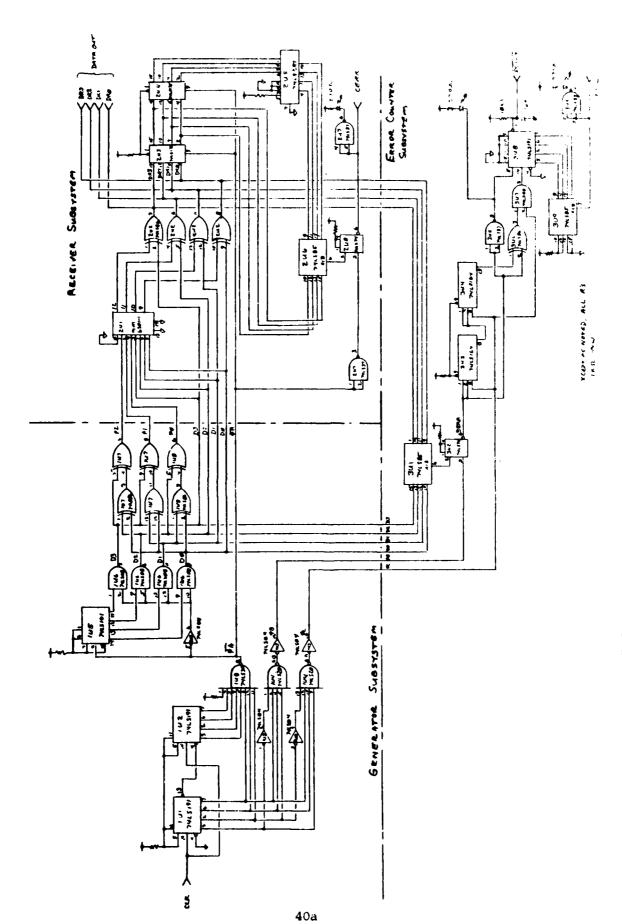
The environmental specification lists the expected signals on the various operating platforms, and at various points per mission. The field would probably be described in terms of the amplitude and deviation about the amplitude of the signals. The modulation to be expected might also be included.

In certain cases of intentional signal spectra, such as communication systems outputs, the specification might include baseband and operating levels. This would enable the use of frequency management if needed to obtain compatibility.

Figure 5-2billustrates a sample page from MIL-HBK-XXXX, mentioned in paragraph 8.1 of the purchase specification. The same guidelines would hold true for conducted emissions at various locations in the platform.

5.2.3 HARDWARE DESCRIPTION

The hardware description would be used by the EMC engineer to determine the effects of the coupled energy, as well as to determine methods of correcting predicted problem areas. The package would consist of schematics, package drawings, block diagrams and timing diagrams. Also included would be tables of standard component responses.



5-1 Rod Control System Schematic

Res Courses System America Mober

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3.0 DESCRIPTION

The function of the RCS is to ensure that all of the control rods in the Generator Containment Fixture (GCF) are utilized equally. This is accomplished by changing the address of the rod to be selected upon receipt of a number of update pulses.

5.0 REQUIREMENTS

5.1 FUNCTION

The RCS shall consist of three subsystems; a generator, a receiver, and an error counter.

5.1.1 GENERATOR SUBSYSTEM

The generator shall accept a pulse train, every 128th pulse of which shall cause a four-bit counter to be incremented. The counter output shall be made available for the receiver subsystem and for the error counter subsystem. Clocking for the receiver and error counter subsystems shall also be provided by the generator subsystem.

5.1.2 RECEIVER SUBSYSTEM

The receiver subsystem shall receive as its input, a fourbit word with appropriate error checking signals. The output of the receiver subsystem shall be a corrected four-bit word to drive the rod selection driver (RSD). The same output is also sent to the pilot's status display (RSD). The corrected output shall also be made available to the error counter subsystem. The receiver subsystem shall also incorporate a sequence error detector to detect non-sequential output addresses. The output of the sequence error detector shall be a logical signal sent to

5.1.3 ERROR COUNTER SUBSYSTEM

The error counter subsystem shall accept the present count from the generator subsystem and the cutuput count from the receiver subsystem. The outputs of the subsystem shall be a bit error indicator, (BEI) which indicates any time the two inputs are in disagreement, and a SCRAM initialize (SCRAM), which will shut down the entier propulsion system whenever the error counter indicates four or more errors in any period of sixteen.

6.1 OUTPUT ERROR SPECIFICATION

In the electromagnetic environment (EME) specified, the output error rates shall not exceed those listed herein.

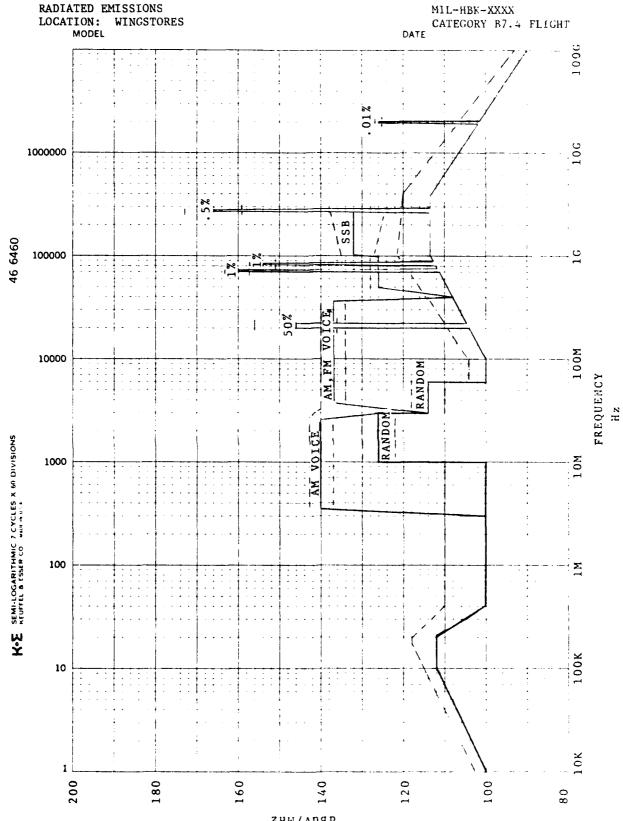
TABLE IV OUTPUT ERROR RATES (EME)

ONE PER 100 HOURS (OPN)	FOUR PER HOUR	TWELVE PER HOUR	ONE PER 1000 HOURS
OUTPUT DATA	SEQUENCE ERROR	DATA ERROR IND (BEI)	SCRAM INITIALIZE

8.1 ELECTROMAGNETIC ENVIRONMENT

The EMI shall be in accordance with MIL-HBK-XXXX, Category B7.4, with the following exceptions.

Flightline	200-300 MHz	50 V/m, am
	1.4-1.8 GHz	200 V/m pk, .001 duty cycle
	9.4 GHz	1.5 kV/m pk, .0001 duty cycle
Takeoff/Landing	200-300 Mhz	10 V/m am
	300-500 MHz	50 V/m, am, 20 kHz fm
	1.4-1.8 GHZ	10 V/m pk, .001 duty cycle
Flight	300-500 MHz	50 V/m, am, 20 kHz fm
	1.4-1.8 GHz	100 V/m pk, .001 duty cycle
	28.4 GHz	1 V/m pk, .001 duty cycle
	16.4 GHz	1 V/m pk, .0001 duty cycle
Mission	2.8 GHz	40 V/m pk, .01 duty cycle
	16.4 GHz	1.2 kV/m pk, .0001 duty cycle
	28.4 GHz	100 V/m pk001 duty cycle



ZHW/ANRP FIGURE 5-2b ENVIRONMENTAL SPECIFICATION 40c

5.3 SYSTEM OUTPUT REQUIREMENTS

The proposed system is examined in light of output requirements as given by the procuring agency. Figure 5-3 shows the input/output relationships between the RCS and other systems, as derived from the purchase specification.

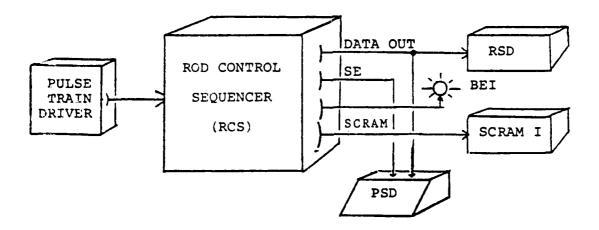


Figure 5-3. Inputs and Outputs of Rod Control System

5.3.1 OUTPUT CLASSIFICATION INDEX

Initialization of EMC control necessitates determining allowable compatibility factor information on all outputs. These compatibility factors must be determined and subsequently tested to meet performance criteria as specified in the purchase specification.

In essence, these compatibility factors are the interpretation of the procuring agency's requirements. They will be the governing specification of the entire EMC portion of system development. Compliance with these factors may be interpreted as follows: if the procuring agency states that output A must have an error rate not exceeding M bit errors/sec, then the compatibility factor derived for that output represents "the probability that output A will not exceed M bit error/sec in its given EME for all desired signals".

The following is a possible OCI on the RCS.

5.3.2 SYSTEM PRIORITY

The Rod Control System description given in the purchase specification Part 3 Section 0 (Figure 6-2) indicates that the loss of system function totally disrupts mission performance. The equipment specification assigns top priority to the system. This is quantized to P=4, by the convention given in Section 3.3.2 of this report.

5.3.3 OUTPUT SEVERITY

The four outputs of the RCS, described in the purchase specification are now analyzed to obtain their given severities.

The severity parameters are determined by interpretation of the proposed system design. Table VII lists the parametric assignments of the four outputs for the three parameters determining Output Classification; redundancy, recoverability and control (see Figure 3-2). Next, the output function effect of each output is judged using the definitions given in Table II of Section 3.

TABLE VII
OUTPUT CLASSIFICATION

<u>o</u>	utput	Redundancy	Recoverability	Control	Totel +1
#1	Data Output	Yes (0)	No (1)	Auto (1)	3
#2	Sequence Error Indicator	No (1)	Yes (0)	Man (0)	2
#3	Bit Error Indicator	Yes (0)	Yes (0)	Man (0)	1
#4	Scram	No (1)	No (1)	Auto (1)	4

Table VIII lists both Output Classification and Output Function Effect entries of the OCI. The value of severity is then read off of Figure 3-3.

TABLE VIII
SEVERITY ASSESSMENT

Output #	Output Function Effect	Output Classification	Severity*
1	3	3	0.66
2	2	2	0.33
3	2	1	0.16
4	4	4	1.0

5.3.4 TOP COMPATIBILITY FACTOR ASSIGNMENT

The formula for assigning compatibility factor for an output based on severity (S) and priority (P) is:

$$C = 1/2 + erf(SxP) \tag{1}$$

as shown in Section 3. The values of compatibility factor for each output, based on severities and priority given earlier, are calculated and listed in Table IX.

TABLE IX
COMPATIBILITY FACTOR ASSIGNMENT

Output #	K= Severity x 4	C= 1/2 + erf(K)
1	2.64	0.9958
2	1.32	0.9066
3	0.64	0.7389
4	4.0	0.999968

^(*) See Figure 3-3.

5.3.5 REQUIREMENTS

The outputs of the RCS must comply with the compatibility factors listed in Table IV for the performance criteria given in the purchase specification.

5.4 FAULT TREE ANALYSIS

The second leg of the analysis on the RCS, is the Fault Tree Analysis (FTA). FTA will be used in allocating the compatibility factors just assigned over lower levels of the system. In this instance, FTA is used to accomplish two tasks:

- Weight subsystem interconnections
- o Allocate compatibility factors to these subsystems.

The organization of this analysis centers around tracing fault potentials that involve any interconnection between the three subsystems. It is assumed throughout the analysis that the engineer has a working knowledge of how these interconnections are utilized in the subsystem layout.

5.4.1 INTERCONNECTION ORGANIZATION

The RCS is organized into three subsystems, as shown in Figure 5-4. For the sake of consistency the following conventions will be used throughout the analysis to label each interconnection:

SYSTEM INPUT

I1 Control pulses

INTRASYSTEM SIGNALS

- X1 position data
- X2 parity data
- X3 clock (ϕ_a)
- X4 clock (ϕ_b) and (ϕ_c)

SYSTEM OUTPUTS

- 01 data out
- O2 sequence error indicator
- 03 bit error indicator
- O4 scram

Table $\, X \,$ shows the organization of the above lines to the subsystem's respective inputs/outputs.

TABLE χ INTERCONNECTION ORGANIZATION FOR EACH SUBSYSTEM IN THE ROD CONTROL SYSTEM

		I 1	X 1	X 2	х3	X 4	01	02	03	04
GENERATOR	Input Output	_ ✓_			-, -	- ,-				
RECEIVER	Input Output		√ 		· -		7 -			
ERROR COUNTER	Input Output						<u>'</u> -		-, -	- ,

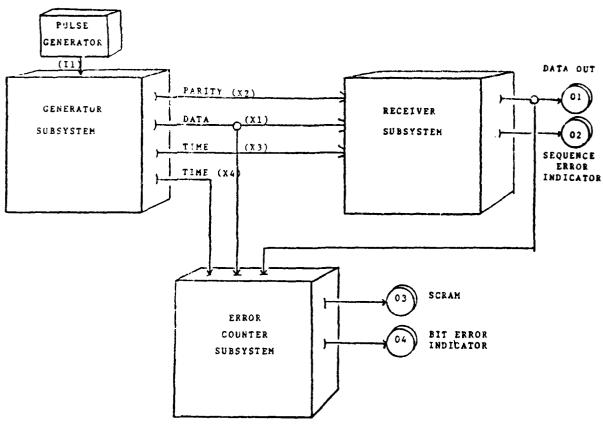


Figure 5-4. Subsystem Functional Diagram

5.4.2 FAULT TREE CONSTRUCTION

The four system outputs have been assigned compatibility factors that must meet all requirements in the purchase specification. Thus, a fault tree must be constructed for each system output (that is, the top fault is that particular system output upset).

Of all the outputs the lowest severity is associated with output 03, bit error indicator. For simplicity, the analysis on this output has been omitted.

Primary faults are assumed to be erroneous signals present on the interconnect lines. In those instances where two or more fault conditions may be associated with the same line, the symbol for that fault condition is primed. Likewise, if the necessary condition of a line is that it be correct, the fault symbol of the line will be barred (example 01 means that the output data is correct).

Three of the interconnect lines have multiple fault conditions: X3, X1 and O1. In the first instance the two fault conditions may be described as:

- x3 Loss of clock signal (due to EMI), or,
- x3' Extra clock signals.

Data lines XI and 01 have the same multiple fault condition associated with them. Because the position data and the output both have four bits, (i.e., can have sixteen positions) there are two special cases of EMI induced upset:

X1, O1 Normally valid data sensed as invalid, X1', O1' invalid data sensed as valid.

Conditions X1 or O1 can occur for any position other than the correct one, the probability of X1 or O1 happening given that an error has occurred is:

15 (possible error positions)

15 (possible error conditions)

or 1.0.

However, conditions X1' or O1' can occur only if an invalid position is sensed as the true position. Therefore, the probability of X1' or O1' happening, given that the fault has occurred is:

1 (possible error position)
----15 (possible error conditions)

or 0.061.

Thus, any weight assigned to conditions X1' or O1' will be one fifteenth that of X1 or O1. This may impact the compatibility factor allocation later on.

5.4.2.1 Fault Tree For Data Output Upset (01)

Two events cause the output data to be upset. The first is that there is an unwarranted continuation of the rods, i.e., for some reason, the rods are advanced when they are not supposed to be. The second event is that the rods fail to increment on command.

Either of these events will cause an upset in the data output, and thus, they must be ORed together in the FTA. The only possible way for either of these conditions to come about, however, is for lines X1 and X2 (data and parity) to be in error simultaneously. In this instance then, either path is accomplished by the ANDing of X1 and X2. The fault tree is shown in Figure 5-5.

The cut sets of the main event are simply (X1, X2) and (X1, X2). As both are the same, there is only one minimal cut set for this fault tree, (X1, X2). The resulting system equation is:

 $01 = (X1) \cdot (X2)$

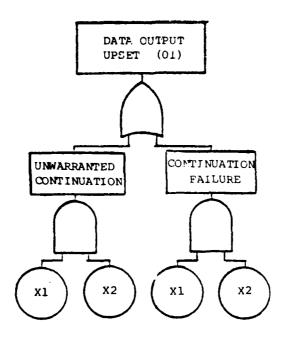


Figure 5-5. Fault Tree for Data Output Upset

5.4.2.2 Fault Tree Sequency Error Indicator Upset (02)

Again there are two events which, when ORed together, result in top fault (O2). They are:

- failure to indicate sequence error
- erroneously indication of a sequence error.

The first event occurs when the timing information is lost (X3) and the output data is incorrect (O1). Therefore, these two conditions are ANDed together. The second event occurs when the clock runs too fast and the data is correct (O1).

Figure 5-6 shows the representative fault tree for the above arguments. The cut sets of this tree are: (X3,01) and (X3,01).

These relationships also represent the minimal cut sets, as there are no redundancies in the cut sets.

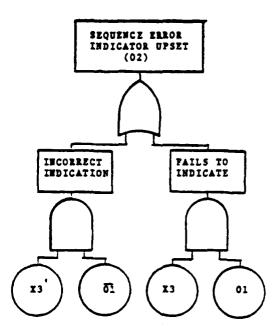


Figure 5-6. FTA for Sequence Error Indicator Upset

5.4.2.3 Fault Tree For Scram Output Upset (04)

Construction of this tree begins by noting that two events can occur to upset the scram output. The first is that the device fails to scram when needed. Three conditions will cause this (all ORed together):

- loss of clock (X4),
- invalid position data sensed as valid (X1'), or
- invalid output data sensed as valid (01').

The second event is that a scram occurs inadvertently. This can only occur if there is a clock, X4. Two faults ANDed with X4 will cause an incorrect scram:

- valid position data sensed incorrectly, or
- valid output data sensed incorrectly.

Figure 5-7 gives the graphical representation of the fault tree associated with these events.

The cut sets for this fault tree are: $(X4, X1^{1}), (O1^{1}), (X4,X1)$ and (X4, O1). This translates to a system equation of

$$04 = (X4) + (X1^{*}) + (01^{*}) + (X4) \cdot (01) + (X4) \cdot (X1)$$

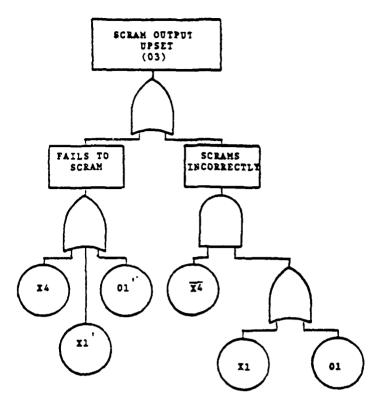


Figure 5-7 FTA for Scram Output Upset

5.4.3 FAULT TREE ANALYSIS APPLICATION

We now have the three equations relating interconnection upset probabilities to system output upsets:

$$01 = (X1) \cdot (X2) \tag{45}$$

$$02 = (x3) \cdot (01) + (x3') \cdot (01) \tag{46}$$

$$04 = (X4) + (X1') + (01') + (\overline{X4}) \cdot (X1) + (\overline{X4}) \cdot (01)$$
 (47)

Note that the equations, as expected, are not independent, as the output (01) is used in both equations (46) and (47). To decouple the equations, the engineering decision is to substitute equation (45) into equations (46),(47). The reason this is an engineering decision is that, from this point on equations (46) and (47) only will be used to allocate compatibility. This is a reasonable assumption as 04 has a much higher assignable compatibility factor than any other output. Equations (46) and (47) therefore, become:

$$02 = (X3) \cdot (X1) \cdot (X2) + (X3^{\dagger}) \cdot (X1) \cdot (X2)$$

$$02 = (X3) \cdot (X1) \cdot (X2) + (X3^{\dagger}) \cdot (X1) + (X3^{\dagger}) \cdot (X2)$$

$$04 = (X4) + (X1^{\dagger}) + [(X1) \cdot (X2)]^{\dagger} + (X4) \cdot (X1) + (X4) \cdot (X1) + (X4) \cdot (X1) \cdot (X2)$$

$$(48)$$

In order to weight the fault conditions, three further assumptions will be made. Primed events in the cut set will have a ranking 1/15 of a normal ranking. As there are six possible fault conditions, (X1, X2, X3, X3, X4, X1'), the ranking factor (1/N) is 0.167. For a complement event (e.g., X1), a ranking factor of (1-0.167 = 0.833).

Lastly, because output events 02 and 04 differ significantly in severity, and the weight of any event is dependent on the sum of all cut set ranks, the rank of all cut sets associated with 02 will be multiplied by 1/3. This represents the ratio of the severity of 02 to the severity of 04.

Table XI calculates the ranking of each cut set, using the above assumptions. For example, cut set 6 has a ranking of:

RANK = (0.167)(0.167)/15

= 0.00185.

The total is divided by 15 because the total is primed.

TABLE XI
CUT SETS AND THEIR RANK

OUTPUT	CUT SET #	MEMBERS	RANK
02	1	x3,x1,x2	0.0015
	2	x3',x1	0.00093
	3	x3',x2	0.00093
03	4	X4	0.167
	5	x1'	0.0111
	6	(X1, X2)'	0.00185
	7	x4,x1	0.139
	8	X4,X1,X2	0.02323
		Total	0.34568

Finally, fault events can be weighted, using Table II. The weight of a fault is defined as the sum of the ranks of all cut sets which contain the faults, divided by the sum of all the cut set rankings. For example, X1 is a member of cut sets 1,2,6,7,8. Therefore, its weight is:

 $W_{X1} = (0.0015 + .00093 + 0.00185 + 0.139 + 0.02323)/0.3654$

 $W_{X1} = 0.48$

Table XII calculates the weights of each fault event.

TABLE XII
FAULT WEIGHT CALCULATIONS

Fault	Member of Cut Set	Weight
хı	1,2,6,7,8	0.48
х2	1,3,6,8	0.10
хз	1	0.004
X4	4,7,8	0.95
x1'	5	0.03
хз'	2,3	0.007

From the above analysis, it is obvious that interconnections X4, X1 are the most critical, whereas, X2 and X3 are of much lower importance. It is important to note that fault condition X1' and X3' are of small concern to the overall system design.

5.4.4 FTA OBSERVATIONS

The last position of the analysis would normally be an allocation of the compatibility factors to the system interconnections, using the techniques outlined in Section 3.4.3. However, if we look closely at equation (47), we observe that X4, X1 and 01 together must be less than 03. X1' and 01' are less a problem than X1 and 01 since they are smaller by a factor of 15. Looking back at the compatibility factor allocation, we see that 04 has a much higher compatibility factor than 01; however equation (3) requires a higher C for 01 than 04. Thus, given the requirements as listed, 01 will have to be improved by at least two orders of magnitude in order for 04 to meet its required C.

A more reasonable approach might be to introduce redundancy, error correction or manual control to output 04, thereby reducing its required Compatibility Factor.

5.4.5 CONCLUSIONS ON FTA

The results of this analysis point out several problems associated with the methodology to date. Perhaps the most evident is the nature of the compatibility factor assignments. As Table III illustrates, a large gap exists in compatibility factors throughout the system. Most importantly, high compatibility factors approach 1.0 quickly. It is hard for the engineer to grasp the difference between C's of 0.99999 and 0.99998. Yet, these numbers arise in the course of an analysis. Clearly, there is a wide gap between the meaning of the "importance" of these two interconnections and their compatibility factors. Yet, this difference is not obvious in the compatibility factors.

A closer look also reveals some of the flaws in the RCS design. For example, if there were a buffer between the data lines going from the generator to both the receiver and error counter, X1 would not require as large a C in the receiver system. Another problem exists in the feedback loop between the data output and the error counter. Again, some buffering of these lines might help in allowing each output attain compatibility.

5.5 EMEA/EMECA

A bottom-up approach provides the EMC engineer with a tool for evaluating the effect of coupled energy at some point in the circuit on the system output. Such a tool is provided by the Electromagnetic Effects Analysis (EMEA) and the Electromagnetic Effect Criticality Analysis (EMECA). The two tools are similar, with the EMECA being an expansion on the EMEA, permitting inclusion of the probability of upset in the analysis. From this, the actual compatibility of the output can be computed for comparison with the required compatibility.

5.5.1 EMEA EXAMPLE

Component compatibility factors are not available; therefore, criticality assessment is not possible, and the following is actually an EMEA. For simplicity, severity is assigned based on the four levels of output function effect, ranging from Catastrophic to Minor.

To reiterate, the Rod Control System consists of three subsystems: the generator subsystem, the error counter subsystem, and the receiver subsystem. Output requirements are specified as follows:

OUTPUT REQUIREMENTS

Data Output

Four pin output giving control rod location from 1-16. Digital output to Rod Selection Driver, and Pilot's Status Display.

A. One error/100 hrs allowable. Severity level critical.

Sequencing Error Check

Visual and digital output whenever a control rod sequencing error has been detected. Digital output to Pilot's Status Display.

B. No redundancy but recoverable. No automatic response. Decision made by knowledgeable crew-member. Up to 4 errors/hr allowable. Severity level major.

Data Error Indicator

Visual indicator only whenever request for positioning information does not agree with actual position.

C. Noncritical, redundant, no automatic response, no action required. Error could result in annoyance and concern for aircraft and crew safety. Up to 12 errors/hr allowable. Severity level minor.

System Fail

Visual and digital output whenever three or more rod positioning errors have been detected in one 16 step sequence. Digital output to SCRAM reactor.

D. One error/1000 hrs allowable. Severity level catastrophic.

This particular EMEA examines each input and output of each component to determine the effect of a "fault" at the system outputs. Faults were considered to be:

- A permanent low state
- A permanent high state
- A transient low state
- A transient high state.

For simplicity, only one failure at a time was considered. A sample page from the EMEA is shown in Figure 5-8.

The component outputs of the EMEA severity assessment were originally color-coded on the schematic ranging from: red for "catastrophic"; yellow for "critical"; green for "major"; blue for "minor"; and uncolored for "unimportant". Overall, the EMEA and the resultant color coded schematic brought to light several significant factors relating to EMC design. In order to facilitate reproduction, however, the method of highlighting has been changed to the width of connecting line. Those lines with higher levels of severity are wider, and those with lower severity are narrower. The marked schematic is shown in figure 5-9.

First, the EMEA points out several areas in which the design itself could be improved to increase reliability of the system. For example, the exclusive OR function at the output to the programmable read only memory (PROM) in the receiver subsystem could have been eliminated by reprogramming the PROM. This would have eliminated four devices and thus increased the system reliability.

Second, the severity flagging immediately shows areas on each subsystem circuit board which could result in "catastrophic" failures if interference were induced on certain interconnect lines. With a color-coded or flagged schematic, circuit board layout personnel could prioritize the PC layout so as to group components and route lines for minimum length (therefore minimum pickup from external fields) in these sensitive areas. This is prominently demonstrated in the generator subsystem clocking circuits and in the error counting circuits.

Third, the flagged lines between subsystems immediately show where extra protection (such as shielding) may be required in the intra-system and inter-system wiring, and where it can be eliminated. In this example data lines between generators and error checking as well as the error counter to receiver subsystems warrent extra protection. The apparent discontinuity in the severity of the generator to receiver interface (from catastrophic to minor) indicates that with proper buffering on the generator side, no shielding would be required.

Fourth, it immediately points out portions of the system that warrant special attention; i.e., areas sensitive to both steady state and transient interference where effects on the system would be "catastrophic" to mission performance. Areas such as the generator counter or the Scram circuit would be examined for possible additional measures such as on board shielding, filtering, or even redesign.

5.5.2 EMECA CONSIDERATIONS

For the EMECA, where criticality is introduced, the initial step is still the EMEA. From this point, it is necessary to calculate pickup on the subsystem wiring from the EME to determine voltage levels at the devices. One of the IAP (Intrasystem Analysis) codes, such as GEMACS could be used for this determination. Next, the device response is determined from known (or measured) device characteristics. Then, the EME environment characteristics are considered, in order to yield component compatibility. Finally, the equation for criticality could be used and component criticalities compiled.

By way of explanation, if for example we have an EME with a distribution E, and a coupling mechanism between the EME and the component with a distribution H, the interfacing signal, I, at the component has a distribution such that:

I = f(E,H).

The resulting interfering signal is then combined with the designed signal, S, and applied to the component whose threshold is described by L.

The compatibility is a function of all three or:

C = g(S,I,L).

This compatibility is then carried through the circuit and compared with the required compatibility at the particular output if the component compatibility is less than the required compatibility, changes are required. Such changes might involve lowering the coupling (H). Utilizing components with a higher threshold (L), or reallocating the individual compatibility factors, as described in paragraph 3.4.5.

FIGURE 5-8

ELECTROMAGNETIC FFFECTS ANALYSIS

SYSTEM: Nuclear Powered Aircraft SUBSYSTEM: Rod Control System MODULE: Generator Subsystem

FUNCTIONAL	FAILURE	EPPECT OF PAILURE	URE I BND EPPECT	EXISTING	LEVEL	REMARKS
1111-1,9,10,15	low	1	non	unused	none	should be tied high
101-4	low spike high	ripple clock would go high disable counters (101+102)	disables whole circuit	none	catas	thru 1k resistor
	high spike	and clock phases (A,B,C) cause counter to miss clock pulse delaying A,B,C	cause circuit to fail to op- erate at proper time	# of pulses needed to get	minor	timing dependent must happen @
102-5,16 102-5,16	low	cause counter (101,102) to reset; inhibit count sequence: disable A.B.C	inhibits normal ckt data xmitted constantly no error checkin	clock pilkas	ratas	depends on what preset input: (c)
	ow spike	set counter to all ones	cause ckt to fail to operate at prescribed time	feedback from PMS	major +	
102-14	nigh 10w	disable count	inhibit Whole ckt operation	none # of pulses	Carrass Binor	
	low spike	pulse; ad	of okt	2		
\$7.00 - 55	10	cause 102 to count with every clock pulse A	cause ckt to fail to operate at prescribed time; data will be xmitted on 16th pulse or not at all	feedback from	Total Total	major depends on state of 101,105 at time of fault
	high	disable counter	ckt will fail to operate DR3-0 always zero; no errors reported (SEI, BEI, SCRAM)	none	catas	
	low spike	cause 102 to count extra clk pulses; A would come early & out of phase	cki will fail to operate at prescribed time; may have data errors	feedback from	major	timing dependent pulse must come at rise of clk; data error due to lack of seithing time between
	9 3 9 9 9	cause counter to miss	ckt will fail to operate at	feedback from	minor	data xmit & datu error check minor data would be
			prescribed time			Xmitted & St
	≱ €	hung low: B on B clk		none	+2	
****	40.	if hang low; I on 3 old ayale	no elk to 342; increase in in clocking; inhibit system fail error		_	_
	Land Spike	cause extra B and/or C pulse	extra clk to 302 and/or ''3	. no.		

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Figure 5-9 EMEA Marked Schematic

RYSBO Amersis Model

SECTION 6

TECHNOLOGY PLANS

- . INTRODUCTION

The methodology presented in the preceding sections forms the framework for a statistical approach to EMC control. It represents a viable alternative to the present deterministic approach by providing prediction analysis and control procedures based on probabilistic criteria. Although a departure from many techniques used by the EMC community, such concepts are already widely used by other engineering disciplines, e.g., Reliability and Safety Engineering. This new methodology addresses microelectronics specifically, yet is applicable to all EMC control situations:

Many areas of the new methodology require further study or refinement before total implementation is possible. It must be understood, however, that important areas such as device response or measurement techniques represent an even greater deficiency to the present deterministic approach. The new methodology allows for the inherent variability of equipments and test methods that is evident but not considered by deterministic means. Fortunately, the deterministic approach has generated many tools which the new methodology may utilize.

As an interim measure, probabilistic criteria for basic elements of the methodology can be assumed. Distributions for device response, EME and coupling models may be approximated from present data. Fault Tree Analysis and EMECAs are already available to control the implementation of these distributions. The time to start utilizing these probabilistic tools is now.

The statistical methodology represents a powerful approach to EMC control. To be maximally effective, however, additional work is required. This section discusses the limitations of the major points of the methodology and presents approaches for their correction. They are presented in decreasing order of significance.

6.2 DEVICE RESPONSE

Predicting Microelectronic based component compatibility requires understanding the response of its basic building block, the microelectronic device. Although there have been significant efforts in this area^{2,3,26} these have dealt primarily with worst-case response to CW signals using relatively simple devices.

The basic process by which EMI induces upset in bipolar devices is through undesired signal rectification at the input junction.^{2,3} At low levels, EMI produces biasing of the junction resulting in timing changes or jitter. At higher levels, the device may latch or toggle depending on the frequency and modulation of the interference. Finally, still higher levels cause device burnout. If the interference is within the passband of the device, the device responds as if the interference were an intended signal. Above device passbands the signal is usually demodulated, with the device then responding to the modulation of the interference.

This process is understood for simple bipolar devices subjected to single interference sources. Typical electromagnetic environments, however, often contain multiple emitters of complex modulations. When these interference signals interact at the non-linearity of the junction, deterministic response analysis becomes next to impossible.

Internal coupling and crosstalk within high density circuitry of modern microelectronic devices is likely. As circuit density becomes higher this problem affects device operation all the more. Again, only very simple cases of crosstalk are addressed presently, and analysis of ever increasing complexity becomes prohibitively expensive.

The basic prediction solution involves following procedures aimed at returning short term answers that assist present approaches but which, over the long-term, culminate in a probabilistic solution. Such a procedure would include:

- Test studies to determine the relevant parameters of the interference/ upset mechanism. Studies must look at the various device families and determine the major interference parameters (e.g. modulation, amplitude, frequency, etc.) causing upset.
- Measurement procedures that allow determination of device parameter values.

Completion of these two steps would greatly augment present technology's ability to predict device operation. With the device response mechanism known at this point, single device response for exact interference levels can be calculated. The problem of device response or interfering level variability must at this time be addressed.

Much of this report has shown that these variabilities are evident in all aspects of EMC based measurements. The solution offered used the concept of compatibility factor as a figure of merit, based upon the statistical distributions of device response, desired signal and interferer.

It is assumed that performance of the above procedures will provide an adequate statistical data base, so that what remains to be done is:

- Develop mathematical models based upon measurment results. Such models
 will include computer simulation or prediction programs, and equations relating the relevant parameters to compatibility factors.
- Develop procedures that use the above models. The final objective is to be able to predict device response as a probability in any environment.

These procedures can only improve the ECM engineer's role in controlling interference in systems utilizing microelectronics. Any increased understanding of device response is desirable because, while great strides are being made in coupling analysis and emitter modelling, the question of how the victim responds to the coupled interference remains largely unanswered.

6.3 LABORATORY EMI MEASUREMENT PROCEDURES AND OBJECTIVES

Under the present MIL-STD-461, -462 scenario, the laboratory EMC test has one prime function; the determination of compliance of a single test sample coupled with a given, deterministic specification. As a result, the knowledge of EMC phenomena so gained tends to be very sparse and the concept of statistical variation ignored. In order to maximize the effectiveness of the EMC test, two areas of change are indicated. The first is an expansion of the present testing to create a useable data base. The second task is a modification and refinement to enable verification of compatibility factor for the population of deliverable components.

MIL-STD-462 describes the basic methods by which emissions and susceptibility of components are measured. For a typical component these measurements are performed once, on a single engineering development model. They are usually performed within the confines of a metallic enclosure of unspecified dimensions. Radiated emissions and susceptibility tests are performed for most frequencies in the near field. Reflections and resonant effects are ignored or inadvertently used to maximize emissions or susceptibility effects. The placement and operation of the component under test and the test transducers are to maximize the emission and susceptibility indications.

The EMI data base for the qualification level components addressed by MIL-STD-462 is not adequate for predicting compatibility at higher levels. Major changes, however, are not immediately required. Significant improvements can be realized with relatively minor changes resulting in a data base more amenable to EMC prediction analysis. These changes would serve as a stop-gap until a complete statistical approach is developed. These suggested changes include:

- Requirements for determining resonant frequencies of the shielded enclosure done on a one time basis this would indicate frequencies at which measured data is questionable; done on a once per test basis would provide specific frequencies of resonance due to room and room-test sample resonances.
- Determination of emission repetition rate by simultaneous peak-quasipeak measurements, or time base measurements using a tuned filter or stectrum analyzer. This would provide data to the system engineer for determining relative potential for interference on a probabilistic basis.
- Requirements to localize and identify source and probable coupling paths
 of above specification emissions and susceptibility would give indications of spacial characteristics of coupling path and of its potential
 severity.
- Detailed modulation characteristics for susceptibility signals would include gate sync'ed and free-running modulations as well as unmodulated test signals to indicate susceptibility probabilities.
- Radiated emission measurements using both loop and rod antennas to 30 MHz
 provide wave impedance data for more accurate coupling predictions

 Broadband, time domain emission measurements - would provide amplitude, duration, repetition rate information needed for digital component EMC prediction

A true statistical approach to EMC will require more significant changes. Measurements will be required on populations of component types in order to determine the distribution curves of the emission and susceptibility characteristics. One question which must be addressed is: how many measurements are needed to satisfactorily determine these distributions? An answer depends on the confidence required in the test data. This requires determining how precisely the compatibility factor must be known.

Test data on individual components will yield point estimates of the true Compatibility Factor. As the number of points increases the Compatibility Factor estimates become more precise and accurate (narrower range). The measured Compatibility Factor is then an estimate within a interval of probable values. The probability (in percent) that the true values lies within this interval is called the confidence level.

Follow-on studies must address these considerations and set bounds on the confidence levels required under given circumstances of component severity and priority. Sampling techniques and automated test methods are also objectives of this study as well as suggestions for further improvements in MIL-STD-462. It is further proposed that this study form the initial basis for determining the basic forms for the distribution curves of typical components.

6.4 COMPUTER AIDED ANALYSIS

Determination of the effects of the EME on component operation brought about the need for special class computer analysis codes. These codes are used to analyze coupling phenomena and device response. Codes useful for device response prediction have been around for several years. Such codes include but are not limited to, ECAP, CODED, TRAC and SPICE. A more recent code is NCAP (Non-Linear Circuit Analysis Program), which is supported by the EMC/IAP support center at RADC.

Coupling model analysis codes are supported much more completely by the EMC/IAP support center. These codes include GEMACS, IEMCAP, the WIRE codes, and PSTAT. These codes are aimed directly at meeting the needs of the EMC community.

As modern electronics passes from analog to digital the need for tools to predict time domain coupling is increasing. This is because digital devices tend to be upset more by peak amplitude than by an integrated energy levels. In order to predict these peak levels, the phase relationships of the spectral components of the interfering signal must be known. This implies Fourier analysis or some yet to be defined code which predicts these levels on a statistical basis.

Implementation of probable models for computers aided prediction will necessitate development of new codes or modification of existing codes to account for variation in coupling or response. Some current codes include Monte Carlo analyses. But such analyses, on a large scale model, are prohibitively expensive. A better approach might be to develop a macro-model system where the distribution of coupling or response is built in.

Some IAP codes also have limitations which restrict their applicability to generalized EMI prediction. A case in point is the program XTALK. As an evaluation, an attempt was made to determine the expected crosstalk on VHSIC (Very High Speed Integrated Circuit) chips. Several changes were deemed desirable from the operational standpoint of the program. The changes included a restructuring of the output format to generate spectral and time domain tables and graphs, and the addition of Fourier and inverse Fourier transform routines. The complex terminating impedances were also redefined to be calculated at each frequency of analysis from a discrete R-L-C network.

In order to model the metalization on the surface of the chip, it was necessary to make several assumptions. First, the dielectric constant of the surrounding medium had to be between that of silicon, the substrate, and air, the adjacent medium. The value taken was the average of the two as a crude approximation. Another assumption had to be made regarding the equivalent size of the conductors. XTALK assumes the conductors are circular in cross section, where in actual practice, the metalization would be rectangular. The difficulty in modeling the metalization comes in determining what diameter round wire gives the equivalent characteristics to rectangular. The decision was made to make the surface areas equal, though the probability of error was still quite high.

Subsequent conversations with Dr. Clayton Paul, the author of XTALK and related codes, revealed another limitation. Due to the phenomenon of charge concentration at close spacing, the XTALK model is accurate only when the spacing between the conductors is ten times or more the wire diameter. This means that for closely spaced conductors, the calculated interwire capacitance is low, leading to errors in calculations. In order to ensure correct results for a variety of spacings, changes in the codes making them more general in application are in order.

Other codes not presently in the IAP, such as those employing bodies of rotation, general theory of diffraction and finite difference time domain analysis, are highly desirable in implementing a probabilistic approach to EMC. These methods permit modeling antennas and structures in areas where the present methods are unreliable or marginally reliable, such as where the structure length approaches half wavelength.

6.5 ELECTROMAGNETIC ENVIRONMENTAL SPECIFICATIONS

In Section 2, development of a compatibility factor hinged upon knowing the device response and interfering source characteristics. Interfering source characteristics involve understanding the electromagnetic environment that an equipment is expected to operate in. 7.1though many references exist describing EMI environments (e.g. MIL-HDBK-235B) deficiencies exist in the proper procedures for mapping these environments into the realm of probability functions.

To overcome deficiencies in understanding of EMI specifications, the following, at a minimum, must be addressed:

- Review of present techniques for measuring environmental levels. Many techniques now used may be applicable to a probabilistic approach.
- e Review of present data bases. Some work has been done on statistical determination of environments. Sailors²⁷ references a man-made noise data base from the Institute for Telecommunication Sciences (ITS). Studying such data bases may allow rapid assimilation of statistical information to present procedures.

• Formulation of statistical data bases. This step comes further in the future, and can be carried out only when device response characteristics (Section 6.2) are better understood.

EMC specification is an important tool in a predesign statistical analysis. It is hoped that already existing data and techniques will allow easy transition from the deterministic to the probabilistic world. Of main concern, therefore, is adapting this data to fit the analysis models gained by the study of device response.

6.6 OUTPUT CLASSIFICATION INDEX

As described in detail in paragraph 3.3, the Output Classification Index (OCI) is intended to standardize the method of setting the Compatibility Factor on the basis of mission profile, system importance, and fault severity. Without a standard technique such as OCI, performance criteria may become arbitrary and fail to consider all aspects of the intended missions. It is imperative, then, that such techniques develop as other areas of study in an EMC methodology progress.

The method given in paragraph 3.3 must be further refined, but is considered a good starting point. Achieving a final OCI procedure will require an iterative study on several systems. This study should proceed along the outline.

- Initial codefication of OCI procedures and parameters. The method proposed in Section 3.3 may be adequate for this step.
- Application of these procedures on different types of systems.
- Correlation of desired results with final results.
- Refinement of OCI codes and procedures.

Such an effort is not unlike many methods use to write standards. The final goal of an output classification index is a flexible, standard technique for assigning higher level EMC performance criteria. These steps are the most straightforward approach for arriving at this goal.

6.7 APPLICATION OF FAULT TREE ANALYSIS TO EMC

The basic concepts of FTA are described in paragraph 3.4. This approach offers the EMC specialist at any level a powerful tool which:

- Assigns priority
- Predicts the probability of compatibility
- Specifies Compatibility Factors at subsystem levels given C at system level
- Provides trade off analysis

A standardized approach to its application is required, techniques presented in Section 3.4 are already practiced by safety engineers.

As other areas of the methodology become better defined, the need for a logical controlling tool will increase. Thus, FTA will become invaluable as the probabilistic approach is phased in. In anticipation of that time, the following should be considered at present, and be implemented as a parallel effort to other studies:

- A step by step procedure for applying the FTA at all applicable levels within typical systems should be determined.
- A determination of cost of the FTA at various levels within the system and of cost versus number of levels covered by the FTA.
- Investigation into computer aided FTA codes. Such codes will aid large, complex system applications.
- Detailed descriptions of limitations (both cost and procedural) of the FTA.
- Cost and Performance trade off study of the FTA applications, considering both manual and computer aided executions.

The merit of FTA is that it functions as a top-down organizational tool. For a probabilistic approach, it will be very useful link between analytical design and final engineering decisions.

6.8 EMECA/EMEA

An approach to the EMECA and EMEA is described in detail in paragraph 3.5. This approach is largely based on the FMECA of Reliability Engineering, modified to address electromagnetically induced faults or "soft failures". Basically, this approach should be refined and standardized so that uniform results could be expected over a variety of users and systems.

Since the EMEA is based on a mature technology, actual implementation is possible at the present. The ability to extend the analysis to include criticalities, however, is dependent upon having compatibility factor data on devices available. As Section 3.5 demonstrated, the EMEA alone is a very valuable tool. The following remains to be examined.

- Cost and performance trade off study of EMEA versus EMECA. A description and rule-of-thumb as to when one approach offers an advantage over the other.
- A determination of cost of the EMECA at various levels within the system and cost versus the number of levels covered by the EMECA.
- A step by step procedure for applying the EMECA at all applicable levels within typical systems.
- Recommendation for a combined approach to EMECA and FMECA when both are applied to the procurement.

The above steps outline the final touches of an EMECA. Since most of the technique is already understood further work will yield large returns in a short amount of time.

SECTION 7

TECHNOLOGICAL FORECAST

7.1 INTRODUCTION

An understanding of where the state-of-the-art in microelectronics is leading over the next four to six years provides an idea of the magnitude of the problem facing the EMC engineer. The direction for proper application of effort in implementing a probabilistic approach to EMC is also revealed through such a study.

There are several areas to be considered, such as which technologies will be dominant, frequencies in the electromagnetic environment, packaging and interconnection methods, and complexities and densities of circuitry. Taken together, they form a picture of the military electronics in the mid 1980s.

7.2 IC TECHNOLOGIES

IC technologies can be divided into three broad categories: bipolar, MOS, and linear. The predominant bipolar technology will be low power Schottky, with ECL limited to high frequencies, and I²L only beginning to emerge into the field. NMOS and HMOS will be the major MOS devices, though CMOS and CMOS/SOS will be taking over an increasingly larger percentage of digital microcircuitry.²⁸ More and more functions previously performed by linear devices will be performed using digital IC's, and an increasing proportion of linear devices will have digital interfaces, both for data and control signals.

By 1985, bubble memory prices will be on a par with equivalent floppy disk systems, and will appear increasingly in military hardware.²⁹ Use of high density memory chips will increase rapidly, including MNOS and CMOS memories.

The use of embedded computers in military systems will be on the rise over the next five years. By 1986, they will account for 36% of the DOD electronics budget. 30

7.3 ELECTROMAGNETIC ENVIRONMENT

The electromagnetic environment is getting more and more cluttered. There have already been several cases of avionics systems that have been qualified to MIL-STD-461A, but have refused to work when installed on the operational platform, until the installation has been "tweaked". Intentional radiators are already in the 18 to 22 GHz frequency range, with an expected upper limit of 100 GHz in the next five years. Switching regulators, with potentially devastating emissions, are operating at 100 kHz, and may be expected to approach 200 kHz by the mid 80s. 34 Microprocessor clocks are already operating in excess of 10 MHz, and can be expected to reach 20 MHz, with resulting harmonic spectra extending beyond 1 GHz.

7.4 PACKAGING AND INTERCONNECTION

As ICs increase in density, the number of pins per package will be on the increase. This will necessitate an increase in the use of leadless chip carriers, with an accompanying increase in signal density on boards and subassemblies. Higher processing speeds will also require closer spacing of components, with a greater

probability of coupling between lines. As a greater emphasis is placed on triservice commonality of equipments, the packaging will have to be effective in a variety of environments.

Weight will also become a critical factor, especially in airborne systems, with a requirement that the packaging designer utilize materials with a high shielding effectiveness to weight ratio. Look for an increase in the use of lightweight composites, as well as more use of commercial grade equipment to reduce costs.

Due to the magnitude of the increase in signals, the interconnections will be forced into an increase in multiplexing. Fiber optics will begin to appear more often by the mid 80s. In order to reduce costs, controlled geometry molded cables, such as ribbon cables, will be used increasingly. This likely will result in higher coupling levels, though it may also permit more accuracy in predicting coupling.

7.5 IC COMPLEXITY AND DENSITY

Integrated circuit complexity has increased markedly over the past decade. Whereas, in 1970, production devices had slightly over 10³ transistors per chip, and advanced devices nearly 4 x 10³, by 1980 production LSI chips had an average of 5 x 10⁴ transistors per chip, while advanced chips were reaching 2 x 10⁵.32 With the VLSI and VHSIC influence, chips with 2 x 10⁵ transistors will probably be fairly commonplace by the mid 80's. In addition to higher density, clock rates of microprocessors are constantly increasing. For example, Zilog has recently anounced a super speed replacement for the Z80, which will be clocking at 12 MHz.³³ Microprocessor chips are handling more and more functions, such as large word length multiply and divide, and large block search and move, as well as incorporating RAMs and ROMs. The RAM on a microcomputer chip can be expected to be in the 1- to 16-k size by the mid 80s, with on-chip ROMs approaching 16- to 64-k.³² Memory chips should be supporting 256- to 512-k.

7.6 IMPACT ON EMC ENGINEERING

The task of developing compatible electronic systems will become increasingly difficult through the 1980s. Frequency spectra, both intentional and unintentional, are increasing, and coupled with the closer spacing of components and interconnections, lead to a much higher coupled interference level. More functions previously performed manually will be automated, increasing the potential severity of upset due to EMI. At the same time, pressure will be increasing to lower costs, reduce weight, and increase the functionality per unit volume. The existing philosophy of deterministic, worst case EMC protection will become so costly and ineffective as to be unusable. A better approach at this time is to introduce to the industry a new methodology for EMI control, a methodology which is dependent on designing to the predicted and actual environment, rather than a parochial specification.

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APPENDIX A

GLOSSARY OF TERMS

APPENDIX A

GLOSSARY OF TERMS

- ACCEPTABLE PERFORMANCE: operation within a range of predefined permissible performance criteria, based upon mission requirements.
- 2. COMPATIBILITY: acceptable performance in the presence of interfering signals.
- 3. COMPATIBILITY FACTOR: the probability that an electronic component will perform acceptably in a given electromagnetic environment for all desired signals.
- 4. COMPONENT: any of the main constituent parts of a system, sub-system, assembly, board, etc.
- 5. DESIRED SIGNALS: those signals which are essential to the operation of a component.
- 6. ELECTROMAGNETIC ENVIRONMENT (EME): all of the electromagnetic signals in a given locale.
- 7. EMI PERFORMANCE CURVE: a plot of a chosen performance criterion vs a function of desired and interfering signal parameters.
- 8. INCOMPATIBILITY: unacceptable performance due to the presence of interfering signals.
- 9. INTERFERING SIGNALS: undesired signals which have coupled into a component. Such signals are referred to as interfering signals even if they do not result in unacceptable performance.
- 10. PERFORMANCE CRITERION: some standard rule or test by which the quality of an equipment can be judged. Examples: bit error rate, articulation index, mean squared error, etc.
- 11. PERFORMANCE THRESHOLD: a value of the performance criterion demarking acceptable and unacceptable performance.
- 12. UNDESIRED SIGNALS: those signals which are not essential to the operation of a component.
- 13. UPSET: occurrence of an undesired event. Example: indicator light erroneously turn on.

APPENDIX B

BIBLIOGRAPHICAL DATA BASE

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MISSION

REPRESENTATION

of Rome Air Development Center

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.

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